Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: Digital Integrated Circuits & Applications [MTE 2105]

REVISED CREDIT SYSTEM
(02/12/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Design MOD-18 negative edge triggered asynchronous up counter **(3M)**

1B. Design of 4:16 line decoder using 2:4 line decoder **(3M)**

1C. Design Full adder using CMOS Technology **(4M)**

2A. A stepper motor drive circuit requires four signal waveforms given in **Fig.Q2(A)** .Design a sequence generator to provide the necessary signals for the stepper-motor drive **(4M)**

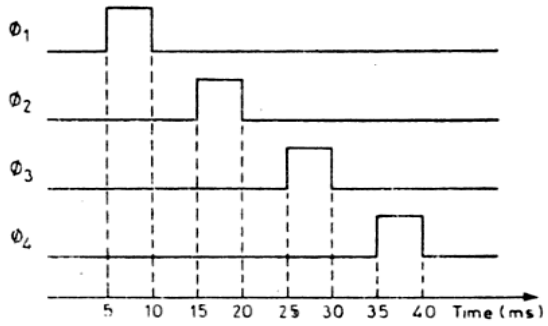


Fig.Q2(A)

2B. An industrial robot that places components on a PCB has 3 fail safe sensors and an emergency shutdown switch. The robot should keep functioning unless any of the following conditions arise: **(3M)**

i) If emergency switch is pressed.
ii) If sensor 1 and sensor 2 are activated at the same time.
iii) If sensor 2 and 3 are activated at the same time.
iv) If all the 3 sensors are activated at the same time.

a) Derive the truth table for the system.
b) Design using K-Map technique a minimum AND – OR gate network for this system.
c) Design the same using minimal NAND gates only.

2C. Identify a device often used in complex digital systems to access a particular memory location based on an "address" produced by a computing device. Hence Implement the functions F1 and F2 using this device and suitable logic gates. Assume that the device has active low outputs: **(3M)**

$$F1\ (A, B, C) = \Sigma\ m(0,2,3,5,6,7)\ ,\ F2\ (A, B, C) = \pi M\ (1,3,4,6,7).$$

3A. Design a synchronous counter for the sequence shown in **Fig.Q3 (A)** using D flip-flop. **(4M)**

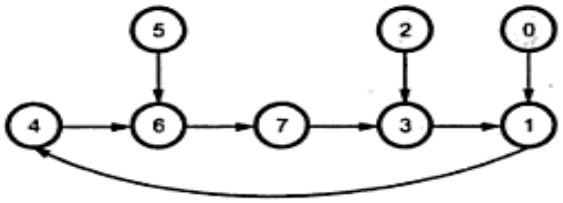
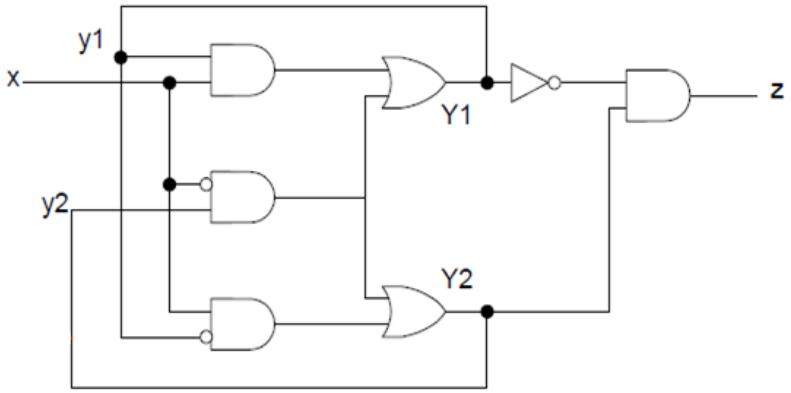


Fig.Q3(A)

3B. Convert T Flip-flop to SR Flip-flop **(3M)**

3C. Analyze the behavior of sequential circuit shown in **Fig.Q3(C)**



(3M)

Fig.Q3(C)

4A. Information bits are encoded on a single line 'X', so as to synchronize with a clock. Bits are encoded so that 3 or more consecutive 1s or, 3 or more consecutive 0s should never appear on the line X. An error indicating sequential circuit is to be designed to indicate an error by generating '1' on the output line z, coinciding with the third of every sequence of three 0s or 1s. For example, if three or more consecutive ones appear, the output remains one for the third and subsequent clock cycles till bit zero is received. **(5M)**
Draw the state diagram for the error detector also Design sequential circuit using D-FF & Mealy machine

4B. Design a 4-bit Binary Parallel Subtractor using 74LS283 IC. Perform subtraction using 2's complement arithmetic and obtain the result in the normal binary form. Hence subtract 9 from 4 using the above block. **(3M)**

4C. Mention no. of clock pulses required for n-bit SISO,SIPO,PISO&PIPO operations **(2M)**

5A. Implement the following four Boolean expressions using three half adders **(3M)**

$$D = A \oplus B \oplus C\,; \quad E = \bar{A}BC + A\bar{B}C\,; \; F = AB\bar{C} + (\bar{A} + \bar{B})C\,; \quad G = ABC$$

5B. Design a mealy network using T Flip-flop that reads as inputs continuous bits, and generates an output of '1' if the sequence (1010) is detected. **(4M)**

5C. For the given expression f(A,B,C,D)= ∑m(0,1,2,4,6,9)+∑d(3,7,10,11,14,15) find Essential prime implicants and minimal expression. **(3M)**