Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DEC/JAN 2017

SUBJECT: Digital Integrated Circuits & Applications [MTE 2105]

REVISED CREDIT SYSTEM

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. **Fig.Q1 (A)** shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

i. The headlights are ON while the ignition is OFF.
ii. The door is open while the ignition is ON.

Implement the logic circuit using only NAND gates. **(3M)**

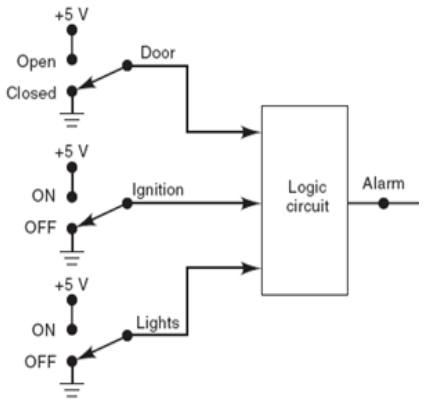


Fig.Q1(A)

1B. Design a half subtractor using CMOS circuit **(4M)**

1C. Simplify the function using 3-variable VEM K-MAP: **(3M)**

$$f(A,B,C,D) = \sum m(0,1,3,5,6,11,13) + \sum d(4,7)$$

2A. Design a BCD adder using 74LS283 IC **(3M)**

2B. Analyze the logic circuit shown in the **Fig.Q2(B)** and find F(A,B,C,D) **(3M)**

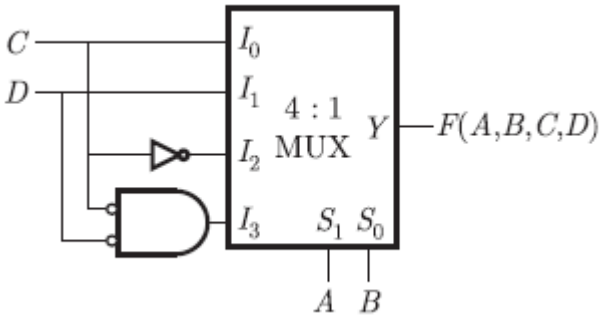
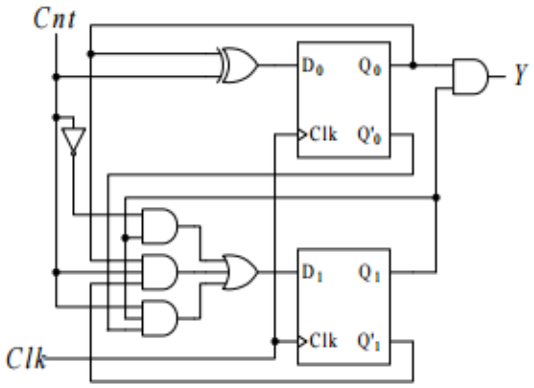


Fig.Q2(B)

2C Derive the next state, the output tables, and the state diagram for the sequential circuit given in **Fig.Q2(C)**



(4M)

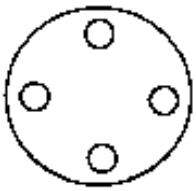
Fig.Q2(C)

3A. Design a 4 bit binary to gray code converter **(4M)**

3B. Design a universal shift register using D flipflop and 4:1 mux IC **(4M)**

3C. Implement a Master Slave flip flop using a 2 to 1 mux **(2M)**

4A. The circle shown in **Fig.Q4 (A)** can rotate clockwise and back. Use minimum hardware to build a circuit to indicate the direction of rotating.



(3M)

Fig.Q4 (A)

4B. Implement the following function using a (i) 8x1 mux (ii) 4x1 mux **(4M)**

F(A, B, C, D)=∑m(0,3,6,9,11,15)

4C. Compare and contrast between moore an mealy machine **(3M)**

5A. Design a 3-bit asynchronous up counter using negative edge triggered JK flip flop. **(3M)**

5B. Realize 1-bit full subtractor using 3:8 decoder (active low outputs) and additional gates **(2M)**

5C. Design a mealy network using D Flip-flop that reads as inputs continuous bits, and generates an output of '1' if the sequence (1011) is detected. **(5M)**