Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2016

SUBJECT: Linear Integrated Circuits & Applications [MTE 2104]

REVISED CREDIT SYSTEM
(30/11/2016)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Find gain of the circuit shown in **Fig.Q1(A)** **(3M)**

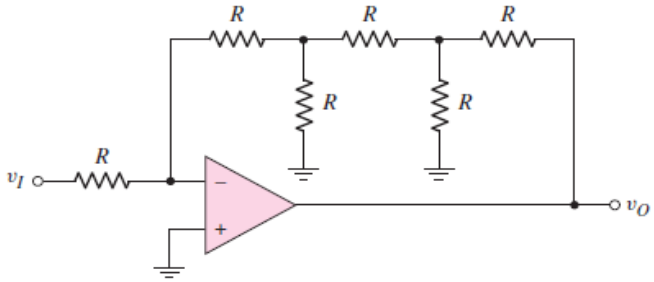

Fig.Q1(A)

1B. Suggest a 4-bit ADC which provides highest accuracy among all ADCs and explain its operation with relevant diagram. **(3M)**

1C. Design -40dB/decade band reject filter having fH = 400 HZ and fL = 2KHZ with a pass band gain of 2. **(4M)**

2A. Design 555 oscillator to produce oscillations with a frequency of 1kHz@50% duty cycle. Connect one RED LED & one GREEN LED so that for 0.5ms the RED LED is ON and GREEN LED is OFF and for next 0.5ms the GREEN LED is ON and RED is OFF. LEDs power supply rating is 5V and 50mA. **(4M)**

2B. Find the value of Ra for the circuit shown in **Fig.Q2(B)** such that $V_2 = \frac{V_3}{3} - 2V_1$ **(3M)**

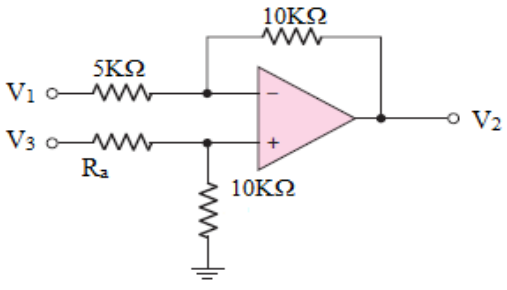

Fig.Q2(B)

2C. Design an op-amp circuit to generate a pulse waveform of frequency 2 kHz **(3M)**

3A. Design a PLL circuit using 565 IC to get:
a) Free running frequency = 10.5 kHz
b) Lock range = 2KHz
c) Capture range = 100Hz **(4M)**
Assume supply voltages of +/- 10V are available. Show pin connection with all component values.

3B. For circuit shown in **Fig.Q3 (B),** R1 = R2 = 10 kΩ, what value of RG will set the gain to 40? **(2M)**

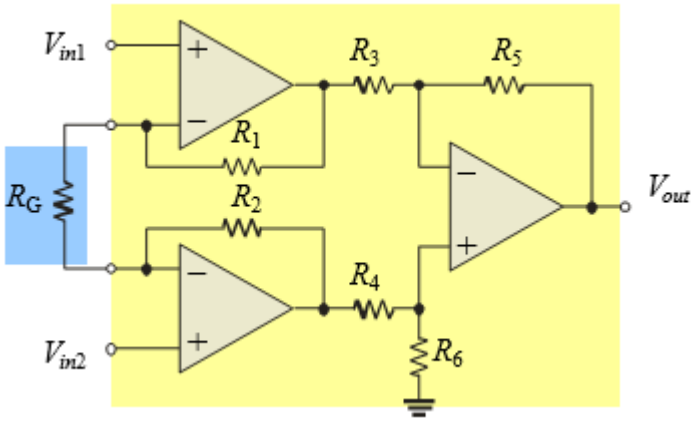

Fig.Q3(B)

3C. Using IC 7805(Three terminal regulator), design a current source to deliver 0.15Amp current to 20Ω, 5 watt load. Draw the functional diagram of LM 317 with protective circuit. (Assume Quiescent current for 7805 is 4.2mA) **(4M)**

4A. Design a non-inverting Schmitt trigger to generate VUTP = -3V, VLTP = +3V **(3M)**

4B. Realize the following second order differential equation using linear Op-Amp applications. **(3M)**

$$\frac{d^2V}{dt^2} + K_1\frac{dV}{dt} + K_2V - V_1 = 0$$

4C. Design 3-bit R-2R ladder type DAC. A 10-bit DAC has step size of 10mv, Find full-scale voltage and % of resolution **(4M)**

5A. Design analog multiplier to multiply two analog input voltages V1 and V2 **(3M)**

5B. Design a circuit to implement $V_0 = 0.545V_3 + 0.273V_4 - 1.25V_1 - 2V_2$ **(3M)**

5C. Design a frequency multiplier circuit using PLL IC 565 to multiply input frequency by 5. Centre frequency is 50KHZ and power supply is ±10V DC. Find lock and capture frequency at output and state related tracking range and capture range limits for input.[Assume C2=100nF, R1=10KΩ] **(4M)**