Reg. No.

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)
END SEMESTER EXAMINATIONS, DEC/JAN 2017

SUBJECT: Linear Integrated Circuits and Applications [MTE 2104]
REVISED CREDIT SYSTEM
Time: 3 Hours   MAX. MARKS: 50

Instructions to Candidates:
- ❖ Answer **ALL** the questions.
- ❖ Missing data may be suitable assumed.

1A. Design an analog divider circuit using 741IC. **4**

1B. Design a timer to switch ON heater for 5 seconds when push button is pressed. **3**

1C. Design an inverting adder circuit using opamp to get the output expression given below. V_1, V_2, V_3 are inputs. Assume $R_f = 10k\Omega$. **3**

$$V_0 = -(0.5V_1 + V_2 + 10V_3)$$

2A. Design a Voltage Controlled Oscillator to produce a free running frequency of 500Hz. $Vcc = 10V$, $R_T = 10k\Omega$, $C_T = 0.1\mu F$. Also estimate **4**
   (i) Variation in free running frequency if Modulating voltage is varied between 7v and 9V. Hence find Voltage to frequency Conversion factor of VCO.
   (ii) Draw the Square wave output if the modulating input is a sine wave.

2B. Demonstrate the working of full wave rectifier using opamp 741. **4**

2C. Elucidate the working of PLL as frequency multiplier **2**

3A. Calculate the output voltage of the circuit shown in **fig.Q3(A)** if $V1 = -V2 = 300mV$ **4**
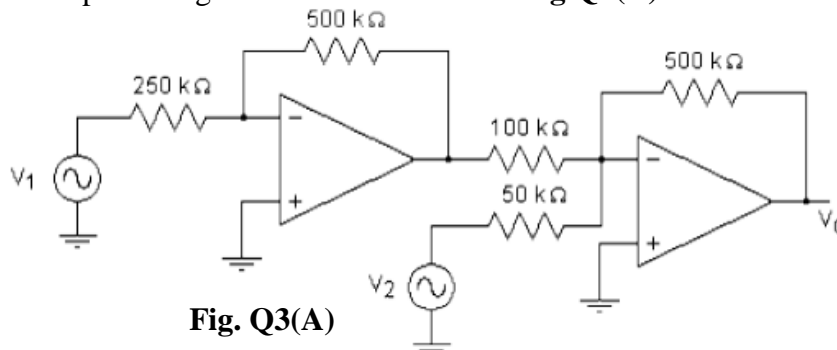

Fig. Q3(A)

3B. Elucidate the working of a Flash type ADC with the help of a 3 bit digital word. **4**

3C. (i) Determine the output voltage of the adjustable regulator shown in **Fig.Q3(C)** **2**
(ii) If R2 is varied from 1KΩ to 10KΩ compute the range of output voltage.
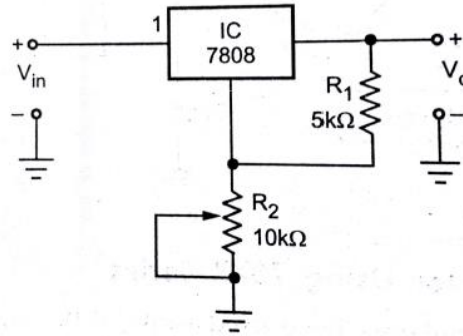(Assume the quiescent current as 100μA)

Fig.Q3(C)

4A. Design a 2nd order Butterworth filter which passes all frequencies between 0 to 1kHz. **6**
Sketch the response of the filter. Assume $C = 0.1\mu F$.

4B. Design a PLL circuit using NE 565 to obtain the free running frequency of 5kHz, **4**
Lock range of 3kHz and capture range of 150Hz. Assume supply voltages of $\pm$ 10V is
available.

5A. Design a Dual slope ADC which uses a 16bit counter and 4MHz clock. Maximum input **4**
voltage is 10V and maximum integrator output voltage is -8V, when counter has cycled
through 2^n counts. Assume $C=0.1\mu F$. Also find the equivalent digital number if the
input is $V_a =4.129V$.

5B. Design a timer using IC 555 to generate a square wave of free running frequency, **3**
10kHZ with 65% duty cycle.

5C. Design following 2nd order Differential Equation using Op-amps **3**
$$5\frac{dV1}{dt} + 7V1 - 3V2 = 0$$