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# MANIPAL UNIVERSITY

## THIRD SEMESTER B.S. (ENGG.) DEGREE EXAMINATION – DECEMBER 2015

### SUBJECT: COMBINATIONAL AND SEQUENTIAL LOGIC (EC 231)

**(BRANCH: CE/CS/E&C/E&E/BIOM.)**

Friday, December 18, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

✍ **Answer any FIVE full questions choosing not more than THREE from ANY unit.**

## UNIT – I

1A. The following numbers with the indicated bases to decimal and hexadecimal:

i) Convert $(1231.23)_{10}$ to hexadecimal.

ii) Convert $(564.73)_8$ to decimal.

iii) Convert $(10110.01110110)_2$ octal.

1B. Given the Boolean function: $(abcd) = a + \bar{a}\bar{b}c + \bar{b}\bar{d}$ . Without minimizing, realize using

i) Two input NAND gates

ii) Two input NOR gates

1C. Solve the following:

i) $(418.59)_{16}$-$(3FB.28)_{16}$ using 16's complement addition

ii) $(1011.0101)_2$-$(110.101)_2$ using 2's complement addition

((2+2+2)+(3+3)+(4+4) = 20 marks)

2A. Simplify the following expressions using Boolean Algebra:

i) $F(abc) = (a + b)(\overline{a} + b + c)(\overline{a} + b + \overline{c})$

ii) $F(ABC) = \overline{A\bar{B} + ABC} + A(B + A\bar{B})(AB + \bar{C})$

iii) $F(xyz) = \overline{x}\,\overline{y}\,\overline{z} + xz + \overline{y}z + xyz$

2B. Convert the following Boolean function $F = (X + Y)(\overline{Y} + XZ)(X + \overline{Z})$ into SOP form canonical SOP form, POS form and canonical POS form.

2C. Explain different self-complementing codes.

((2+2+2)+8+6 = 20 marks)

3A. Design BCD to Excess 3 converter using minimum logic gates.

3B. Design Full adder using NAND gates.

3C. Realize the function $f(abcd) = \pi(0,2,5,7,8,9,13,14,15)$ using 8x1 multiplexer use lower inputs as select lines.

(12+4+4 = 20 marks)

4A. Implement16 to 1 multiplexer using 2 to 1 multiplexers.

4B. Simplify the following Boolean functions using k-maps and realize using logic gates.

i) $f(A,B,C,D) = \sum m(1,2,3,4,6,8,9,10,11)$

ii) $f(W,X,Y,Z) = \pi M(1,5,6,7,11,12,13,15)$

4C. Using 2 to 4 decoders with enable, implement 4 to 16 decoder as a max term generator.

(6+(4+4)+6 = 20 marks)

## UNIT-II

5A. With syntax define the following terms with respect to VHDL:

i) Entity

ii) Architecture

iii) Signal

5B. Explain different types of RAM and ROM.

5C. Write a VHDL code for 4 to 1 multiplexer.

(6+8+6 = 20 marks)

6A. Derive characteristic equations for SR, JK, T and D flipflops.

6B. Design synchronous mod16 down counter using JK flipflops and draw the timing diagram.

(10+10 = 20 marks)

7A Explain the universal shift register.

7B. Using JK flipflops, with negative edge triggered clock Design mod 16 ripple counter which can be controlled to count up or down.

7C. Design four bit Ring counter using D-flipflops. Draw the timing diagram.

(8+8+4 = 20 marks)

8A. Design Mod 12 asynchronous up counter using JK flipflops. Also draw the timing diagram.

8B. Implement following Boolean functions using Programmable Logic array:

$f1(a,b,c) = \sum(0,1,2,5,7)$, $f2(a,b,c) = \sum(1,2,4,6)$

8C. Explain the operation of Master slave JK flipflop with timing diagram.

(8+8+4 = 20 marks)