Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
(A Constituent Institute of Manipal University)
Manipal – 576 104

THIRD SEMESTER B.Tech (BME) DEGREE END-SEM EXAMINATIONS – NOV/DEC 2015
SUBJECT: ANALOG ELECTRONICS (BME 2102)
Thursday, November 26, 2015 (9.00 a.m. - 12.00 noon)

DURATION: 3 HOURS **MAX. MARKS: 100**

Instruction to Candidates:

Answer all FIVE full questions.
Assume relevant data if missing.
Give diagrams wherever necessary.

1A	The amplifier circuit in the figure 1A is designed in such a way as to have an operating point of 6V, 1 mA. If the transistor has β =150, find R_E, R_C, R_1 & R_2. Assume $V_{BE} = 0.7V$.	**8**
1B.	What do you understand by transistor biasing? What is its need? Mention various methods of biasing stating their advantages and disadvantages. How stabilization of operating point is achieved by potential divider method?	**6**
1C.	Draw the small signal model of common collector configuration and express common collector hybrid parameters in terms of common emitter hybrid parameters.	**6**
2A.	Consider acquiring an ECG signal in a lab environment. The circuit of a common source FET amplifier as shown in the figure 2A is acting as a pre-amplifier. Find expressions for voltage gain A_V and current gain A_I for the circuit in mid frequency region where R_S is bypassed by C_S. Find also the input resistance for the amplifier. If R_D = 3kΩ, R_G = 500kΩ, μ = 60, $r_d = 30K\Omega$, compute the value of A_V, A_I, and input resistance.	**8**
2B.	There is a need for amplification of epileptic EEG signal in order to give it to an analog to digital converter. The basic amplifier is required to boost the signal to a certain level. For this basic amplifier, derive the general formula for the following parameters: (*i*) Input impedance (*ii*) current gain (iii) output impedance and (*iii*) voltage gain in terms of *h* parameters and the load.	**6**
2C.	A germanium bipolar junction transistor has $hie = 6K\Omega$ and $h_{fe} = 224$ at	**6**

	$I_C = 1mA$ with $f_T = 80MHz$ and $C_{b'c} = 12pF$. Determine g_m, $r_{bb'}$, $r_{b'e}$ and $C_{b'e}$ at room temperature.	
3A.	An RC-coupled amplifier stage uses an FET with $\mu = 70, r_d = 44K\Omega$, $R_D = 50K\Omega$, $R_g = 1M\Omega$. Assume a total shunting capacitance of 100pF. Find mid band amplification in dB's, upper 3-dB frequency and capacitance C_b if $f_L = 50Hz$.	**8**
3B.	What do you understand by multistage transistor amplifier? Mention its need and the different types of inter-stage coupling incorporated into the circuit. How will you achieve impedance matching with transformer coupling?	**6**
3C.	What will be the effect of emitter bypass capacitor on the low frequency response of a multi-stage amplifier? Provide suitable expression for the lower 3-dB frequency and its relation with the pole frequency.	**6**
4A.	An amplifier with un bypassed emitter resistance have an overall trans conductance gain of $-1mA/V$, voltage gain of -4 and $D = 50$. If $R_S = 1K\Omega$, $h_{fe} = 150$, Find R_e, R_L and R_{if}.	**8**
4B.	Illustrate the effect of negative feedback on the input and output resistances of a current series feedback amplifier. Justify by providing suitable expressions.	**6**
4C.	Find $\frac{V_{f'}}{V_o}$ for the network shown in Fig 4B. Determine the expression for the frequency of oscillation and find the minimum gain required for oscillation. Draw the FET phase shift oscillator.	**6**
5A.	Design a suitable circuit that is required to generate sinusoidal oscillations in the radio frequency range. Assume stability factor of the circuit to be 6.	**8**
5B.	How does push pull configuration help in reducing nonlinear distortion in class B power amplifier? Justify the same with suitable circuit and characteristics. Defining ac output power and dc input power, arrive at an expression for the maximum collector power dissipation.	**6**
5C.	Draw the circuit diagram of common source amplifier using depletion MOSFET with the following circuit components. $R_D = 6.2k\Omega, R_G = 1M\Omega$, $R_S = 2.4k\Omega, I_{DSS} = 8mA \& V_P = -8V$. Determine the operating point, V_D, ac equivalent circuit, input impedance and output impedance.	**6**

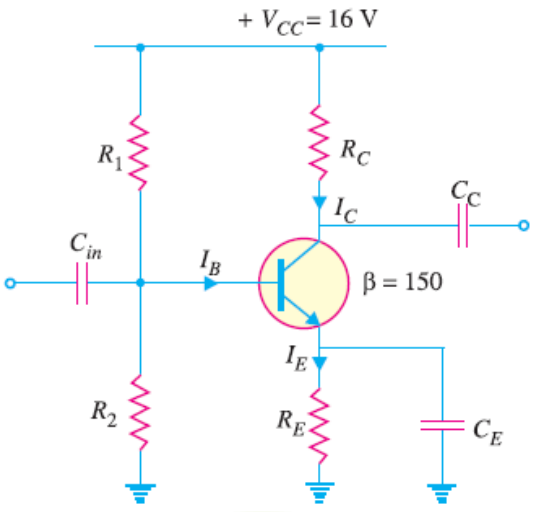

Fig 1A

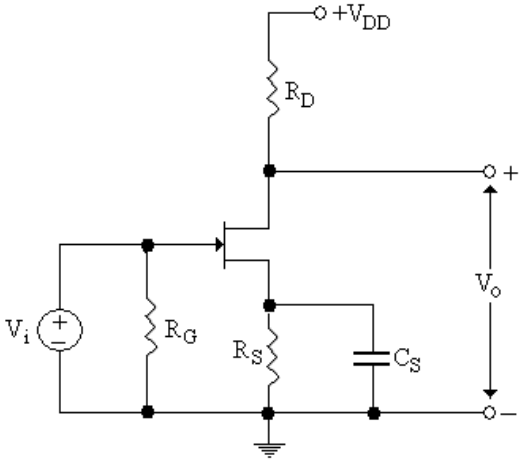

Fig 2A

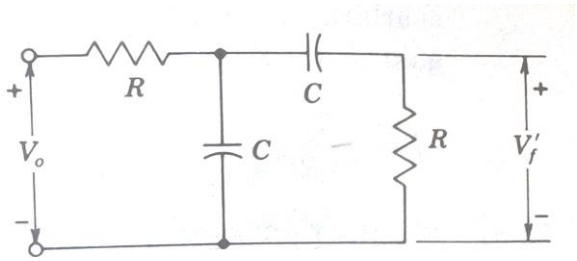

Fig 4B