Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
(A Constituent Institute of Manipal University)
Manipal – 576 104

III SEMESTER B.Tech (BME) DEGREE MAKEUP EXAMINATIONS, DEC / JAN 2015-16
SUBJECT: DIGITAL ELECTRONICS (BME 2103)
(REVISED CREDIT SYSTEM)
Tuesday, January 05, 2016: 9.00 a.m. – 12 Noon.

TIME: 3 HOURS **MAX. MARKS: 100**

Instruction to Candidates:
Answer ALL the questions.

1. A. Design a decoder circuit for common cathode seven segment display to display decimal numbers from 0 to 3. (08)

   B. (a) Define a digital Multiplexer. (08)

   (b) Realize the Boolean function $f(A\ B\ C\ D) = A\bar{B}C + \bar{B}C\bar{D} + AC + \bar{B}D$ using 8x1 Multiplexer.

   C. Construct the state diagram for a Mealy sequencial circuit that will detect a sequence "110" from an input sequence. (04)

2. A. Simplify the following Boolean function using "Quine McCluskey" method: (08)

   $f(A, B, C, D) = \sum m\ (0, 2, 3, 6, 7, 8, 10, 12, 13)$

   B. (a) Design a Mod-10 Ripple counter using JK Flip-flops. (08)

   (b) A 4-bit synchronous counter uses flip-flops with propagation delay of 25ns each. What is the maximum possible time required for change of state?

   (c) What is the output frequency of a Mod-16 counter, clocked from a 20kHz clock pulse?

   C. Convert JK Flip-flop to D Flip-flop. (04)

3. A. What is a Shift Register? Design a 4-bit Serial-in Serial-out (SISO) / Serial-in Parallel-out (SIPO) Shift Register using D Flip-flops. (08)

   B. Simplify the following Boolean function using "Karnaugh Map": (08)

   F (w, x, y, z) = $\sum$ m (1, 3, 7, 11, 15) + $\sum$ d (0, 2, 5)

C. What is a digital comparator? Design a 1-bit digital comparator. (04)

4. A. Illustrate the design of a Moore sequencial circuit, by designing a sequence detector which will detect an overlapping sequence "101" from an input sequence. (08)

B. Design a 4-bit Adder-Subtractor circuit. (08)

C. Perform the following subtractions using 1's and 2's complements. (04)

(a) $11010_2 - 1101_2$ (b) $100_2 - 11000_2$

5. A. Design a 3-bit synchronous counter using JK F/Fs. (08)

B. What is a parity bit? Mention its significance. Design a 3-bit Odd-parity Generator / Checker. (08)

C. Perform the following decimal additions in the 8421 code. (04)

(a) 88.6 + 12.3 (b) 679.6 + 536.8

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