Reg. No.										

प्रज्ञानं ब्रह्म

Manipal
INSPIRED BY LIFE

MANIPAL INSTITUTE OF TECHNOLOGY, MANIPAL 576104

(Constituent College of Manipal University)

THIRD SEMESTER B. TECH. (CCE) DEGREE END SEMESTER EXAMINATION, NOV/DEC – 2015
SUBJECT: DIGITAL SYSTEM DESIGN – ICT 2151
(REVISED CREDIT SYSTEM)

TIME: 3 HOURS **28/11/2015** **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data, if any, may be suitably assumed.

1A. Design a hardwired control unit for 4x4 Booth's multiplier.
1B. Convert a given D – flip flop to work as JK – flip flop.
1C. Design a full subtractor using two half subtractors and one OR gate.

[5+3+2]

2A. Design a sequence detector with one input X and one output Y. The output Y is HIGH whenever the sequence "010110" is detected. Otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using T- flip flops and minimum number of external gates.
2B. Given M = - $4_{(10)}$ and Q = - $6_{(10)}$, multiply using Booth's Algorithm indicating all the steps.
2C. For a MOD – 6 Johnson counter show that decoding can be done using 2 – input AND gates only.

[5+3+2]

3A. Using 7493 ICs, 7485 ICs and minimum number of external gates, design a 2-digit BCD up counter to count from 0 to N.
3B. With a neat logic diagram, explain the operation of 16×16 Barrel shifter which is capable of rotating the given 16 bit data to the left by 'n' positions, where $0 \le n \le 15$.
3C. Design 4 to 2 priority encoder using basic gates.

[5+3+2]

4A. Design 4 – bit × 4 – bit binary multiplier using 7483 ICs and minimum number of external NAND gates.
4B. Using 74153 IC and external NAND gates, design the combinational logic circuit to implement the following functions:

$F_1(A,B,C) = \overline{A}\,\overline{B} + AB\overline{C}$

$F_2(A,B,C) = \overline{A} + B$

4C. Explain address translation mechanism for a paged segmentation system.

[5+3+2]

5A. Design a self starting synchronous counter to count the BCD digits according to 8 4 -2 -1 code. Use SR – flip flops for the design with minimal external gates.
5B. Design a 4 to 16 decoder using 2 to 4 decoders ONLY.
5C. Explain the principle of operation of set associative mapped cache with an appropriate example.

[5+3+2]