Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY, MANIPAL 576104

(Constituent College of Manipal University)

THIRD SEMESTER B. TECH. (CCE) DEGREE MAKE UP EXAMINATION, JAN – 2016

SUBJECT: DIGITAL SYSTEM DESIGN – ICT 253

(REVISED CREDIT SYSTEM)

TIME: 3 HOURS **01/01/2016** **MAX. MARKS: 50**

Instructions to candidates

- Answer any FIVE questions.
- Missing data, if any, may be suitably assumed.

1A. Design a sequence detector with one input Y and one output Z. The output Z is HIGH whenever the sequence "110101" is detected. Otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using D- flip flops and minimum external gates.

1B. Using 74138 IC and external NAND gates, design the combinational circuit to implement following functions:

$F_1(A,B,C) = \bar{A} + A\bar{C}$

$F_2(A,B,C) = \bar{A} + BC$

$F_3(A,B,C) = A\bar{B} + \bar{A}B$

1C. What is the role of TLB in virtual address translation?

[5+3+2]

2A. Design a code converter to convert a decimal digit represented in Excess-3 to decimal digit represented in 8 4 -2 -1 code, using NAND gates only.

2B. What is Race around Condition in JK – Flip Flop? With necessary diagrams, explain how master–slave JK – flip flop overcomes the same.

2C. Explain the principle of operation of direct mapped cache with an appropriate example.

[5+3+2]

3A. Design a microprogrammed control unit for 4x4 Booth's multiplier.

3B. Design a 32 : 1 MUX using 4 : 1 MUXs ONLY.

3C. Design MOD – 8 Johnson counter using D – flip flops. Write the counting sequence.

[5+3+2]

4A. Design a self starting synchronous counter using JK – flip flops and external gates to count the sequence $1 \rightarrow 3 \rightarrow 6 \rightarrow 9 \rightarrow 12 \rightarrow 5 \rightarrow 1$.

4B. Given $M = -5_{(10)}$ and $Q = 7_{(10)}$, multiply the two numbers using Booth's Algorithm. Indicate all the steps.

4C. Design a logic circuit which divides the frequency of the input square wave by a factor of '12' while producing an output waveform with 50 percent duty cycle.

[5+3+2]

5A. Using 74193 ICs, 7485 ICs and minimum number of external gates, design an 8-bit binary down counter to count from N1 to N2 where N1 > N2.

5B. Design a carry save adder to add four 3- bit signed numbers using full adders.

5C. Design 1 – bit magnitude comparator with cascading inputs using NOR gates only.

[5+3+2]

6A. Design a 4 – bit ALU to perform the following operations:

S_1	S_0	F
0	0	A+B+1
0	1	A-B
1	0	A XOR B
1	1	A NAND B

Where A, B, F are 4 – bit numbers.

6B. Design 4 – bit adder/ subtractor using 7483 IC and 2:1 MUXs only.

6C. Design a 3 – bit × 2 – bit binary multiplier using full adders and external AND gates only.

[5+3+2]