Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: COMPUTER ORGANIZATION AND DESIGN [CSE 201]

Time: 3 Hours 26-11-2015 MAX. MARKS: 50

Instructions to Candidates:

- Answer any FIVE full questions.
- Missing data, if any, may be suitably assumed.

1A. Explain the connection between processor and memory with the help of a neat diagram, highlighting the roles of various registers involved. 4M

1B. Explain register direct and register indirect addressing modes with syntax and examples. 3M

1C. Explain the working of Carry Lookahead Adder(CLA). Derive the total number of gate delays required to generate S_{11} in a 16 bit Adder designed by cascading four 4-bit CLAs. 3M

2A. What is booths recoding of multiplier? Demonstrate multiplication of 13 with -6 using the same. 3M

2B. CSAs enable fast multiplication. Justify this statement with explanation and appropriate diagrams. 3M

2C. What is the need for guard bits in floating point operation? What are the different methods of truncating the final result? 4M

3A. For the state diagram given in Fig. 3A, design the final controller diagram (hardwired) using D-Flip Flop and a PLA and show controller's state table for PLA(ignore the control points) 4M

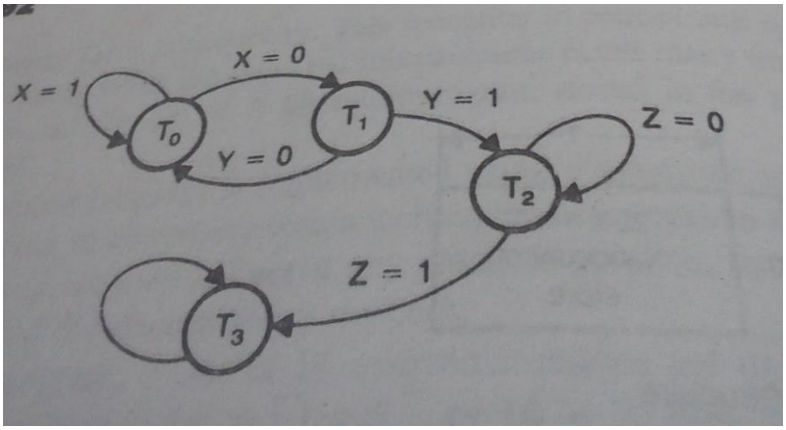

Fig 3A

3B. For the Register Transfer Description given below, identify the micro-operations and derive the size of the control memory required for micro-programmed control unit. Using this information design the micro-programmed control unit.

```
        Declare registers A[4], B[4], C[4];
        Declare inbus[4],outbus[4];
START:  B←inbus, A←0;
        C←inbus;
LOOP:   if B>C, go to SUB;
        A←B+C;
        Go to JUMP;
SUB:    A←B-C;
JUMP:   B←B-1;
        If B>0, go to LOOP
        Outbus←A;
```

3M

3C. Show the control memory contents for Q.3B. 3M

4A. A certain word addressable main memory is addressable by an 8 bit address and has 16 blocks. Cache memory consists of 8 blocks and the block size is similar to that of main memory. With the help of memory block diagram, explain splitting of address in direct , associative and set associative(2 blocks) mapping functions of cache for the above memory assumptions. 4M

4B. Explain hit rate, miss rate and miss penalty of cache. Using this, derive equation for average time to access main memory when two levels of cache is used. 4M

4C. Explain "cycle stealing" and "bus arbitration" concept associated with DMA. 2M

5A. How is read and write achieved in magnetic hard disks? 2M

5B. Explain the 1-bus and 2-bus architecture. 4M

5C. What is the need for virtual memory? With the help of a diagram, briefly explain its address translation process. 4M

6A. What is Direct Memory Access(DMA)? Explain the sequence of events involved during data transfer using DMA. 3M

6B. How is synchronizing data transfer using interrupts different from that of polling? 2M

6C. With the help of diagrams, illustrate the interrupt handling using individual interrupt request lines and daisy chain method. 5M