Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (COMPUTER SCIENCE AND ENGINEERING)

MAKE UP EXAMINATIONS, DEC 2015/JAN 2016

SUBJECT: COMPUTER ORGANIZATION AND DESIGN [CSE 2101]

REVISED CREDIT SYSTEM

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Write 8-bit 1s and 2s complement representations for
(i) -1 (ii) -99 **2M**

1B. Write a CISC program to add an array of 10 numbers. The 10 numbers are stored in a memory which is byte addressable. Each number occupies a word and one word is 4 bytes in length. **3M**

1C. With a neat sketch, discuss the five functionally independent parts of a computer. **5M**

2A. (i) Draw the diagram of RMW unit and write down the register transfer description for memory read and memory write. **2M**
(ii) Write example multiplier for best and worst cases of booth's algorithm. **1M**

2B. (i) Write down the restoring division algorithm. **2M**
(ii) What is the meaning of following register transfer descriptions?
(a) A[0]←B[2] (b) LSL(A$B) where A and B are 4-bit registers **1M**

2C. Consider a 12-bit floating-point number representation format wherein the first bit is the sign of the number, the next five bits represent an excess 15 exponent for the scale factor, which has an implied base of 2 and the last six bits represent the fractional part of the mantissa, which has an implied 1 to the left of the binary point. Given below are 2 floating point numbers represented in the above mentioned format.

A=	0	10001	011011
B=	1	01111	101010

Multiply A by B. Use booth's multiplication algorithm to multiply the mantissas of A and B. **4M**

3A. Consider the following register transfer description

Declare registers A[8], B[8], C[8], D[8], T[1];
Declare buses inbus1[7], inbus2[7], outbus[7];
Start: A[6:0]←inbus1, B[6:0]←inbus2, A[7]←0, B[7]←0, D←0,T←0;
C[6:0]←inbus1, C[7]←0;
D←A-B;
T[0]←D[7];
If T[0]=0 then D←A;
If T[0]=1 then D←B;
D←D-C;
T[0]←D[7];
If T[0]=1 then outbus=C[6:0];
If T[0]=0 then outbus=D[6:0];
Halt: Go to Halt;

(i) Draw the state diagram. **2M**

(ii) Write the sequence controller truth table and boolean equations for the outputs of sequence controller. **2M**

3B. For register transfer description given in Q3A, design the micro-programmed control unit. Use fully encoded format for condition select, branch address and control functions fields. **3M**

3C. Answer the following:

(i) Write any 4 differences between hardwired and micro-programmed approach. **1M**

(ii) With a neat diagram, explain one-bus organization. **2M**

4A. (i) Draw typical ROM cell and explain PROM. **2M**

(ii) Write short notes on

a) EPROM.

b) Flash drives, its advantages and disadvantages. **2M**

4B. Suppose that cache has only 8 blocks and each block can have only one word. Accordingly the main memory is divided into blocks, each block having only one word. Memory is word addressable with 16-bit address. A 10*10 array of numbers (A) each occupying one word is stored in memory locations 5A00 to 5A63. Another 10*10 array of numbers (B) each occupying one word is stored in memory locations 7B00 to 7B63. The elements of these arrays are stored in row order. SUM, SUM1, i, j, AVE, AVE1 are held in processor registers. The replacement algorithm to be used is LRU.

Consider the task

```
SUM:=0
SUM1:=0
for j:=0 to 9 do
SUM:=SUM+A(j,0)
SUM1:=SUM1+B(0,j)
end
AVE:=SUM/10
AVE1:=SUM1/10
for i:=9 to 0 do
B(0,i):=B(0,i)/AVE1
A(i,0):=A(i,0)/AVE
end
```

For the task given, trace the contents of cache iteration after iteration for both j loop, i loop for Associative mapped cache. Calculate the total number of cache hits and cache misses. **3M**

4C. For the task given in Q4B, trace the contents of cache iteration after iteration for j loop only for Set-associative mapped cache (2-way set associative). Calculate the total number of cache misses. . **3M**

5A. Write in detail about CD-Rewritable. **3M**

5B. With a neat diagram, discuss display to processor connection. **3M**

5C. Answer the following:

(i) Suppose let's say processor receives an interrupt request during execution of instruction 'i' in program 'p'. With a neat sketch, explain what the processor will do to handle the interrupt request. **2M**

(ii) Draw the diagram of connection for processor, keyboard, display. **2M**