Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: COMPUTER ORGANIZATION AND DESIGN [CSE 2101]

REVISED CREDIT SYSTEM
DATE: 26-11-2015

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Convert the following pairs of decimal numbers to 4-bit 2's-complement numbers, then add them. State whether or not overflow occurs in each case.

a) -3 and -7 b) -7 and 1

Repeat for the subtract operation using 2's complement method, where the second number of each pair is to be subtracted from the first number. State whether or not overflow occurs in each case. 2M

1B. A computer is having 32-bit word length and the memory is byte addressable. Discuss on Instruction execution and straight-line sequencing for the task C=A+B. Use a possible program segment for this task as it appears in the memory of a computer. 4M

1C. Explain with syntax and examples any two addressing modes supported by CISC but not supported by RISC. 4M

2A. Design a 4-bit, ALU with the following specifications:

S1	S0	function to be performed
0	0	A plus B
0	1	B
1	0	A OR B
1	1	A'

5M

2B. Write down the rules involved in subtraction and multiplication of two floating point numbers. Consider the following 12-bit floating-point number representation format. The first bit is the sign of the number. The next five bits represent an excess 15 exponent for the scale factor which has an implied base of 2. The last six bits represent the fractional part of the mantissa, which has an implied 1 to the left of the binary point. Represent the number in binary and then perform A minus B and A multiply B operations on the operands. 5M

A =	0	10001	011011
B =	1	01111	101010

3A. List all the steps involved in the design of hardwired control unit. 2M

3B. Write a register transfer description for 4 X 4 unsigned sequential multiplier. Here Q register is initialized with the multiplier, M register with multiplicand and L register holds iteration count. Note that these registers need to be initialized through inbus. 4M

3C. Give the comparison on

a) horizontal versus vertical micro instructions

b) Hardwired Control unit versus microprogrammed Control unit 4M

4A. Explain in detail how the Write buffer supports in enhancing the performance of a computer when write-through and write-back protocols are used. 5M

4B. A cache consists of 64 blocks, and the main memory contains 4096 blocks, each consisting of 128 words.

a) How many bits are there in a main memory address?

b) How many bits are there in each of TAG/SET/WORD field in direct mapping and associative mapping? Show your calculation with appropriate diagrams. 5M

5A. Define the terms: Page, Page table, Page frame, Page table base register. 2M

5B. Explain with neat diagram the use of Associative mapped TLB in address translation from virtual address into physical address. 4M

5C. With the supporting diagram for keyboard to processor connection explain the functioning of input interface. 4M