Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: SWITCHING CIRCUITS AND LOGIC DESIGN [CSE 2102]

REVISED CREDIT SYSTEM

Time: 3 Hours 28-11-2015 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Let X and Y are 2 bit numbers with $X=x_1x_0$ and $Y = y_1y_0$. Design a circuit with X and Y as inputs and produces an output f such that f should be 1 only if X > Y. Otherwise f should be 0.

a) Show the truth table for f
b) Show the simplest possible SOP expression for f using algebraic manipulation
c) Design the circuit using basic gates
d) Implement this design using NAND gates only 4M

1B. Derive the simplest POS expression for the following function using algebraic manipulation. Implement this using only NOR gates.

$f(a,b,c,d,e) = (b' + c + e)\ (a + c' + e)\ (a + b + e)\ (a+ d' + e')$ 3M

1C. Use KMap to find the minimum cost SOP expression for the function

$f(w, x, y, z) = wxy + yz + xy'z + x'y$

Write the prime implicants and essential prime implicants. Implement the circuit using NOR gates only. 3M

2A. Use functional decomposition to find the best implementation of the function

$f(A,B,C,D) = \prod M(1, 2, 3, 7, 8, 12, 13, 14)$

Draw the logic diagram for your implementation assuming that the input variables are available in uncomplemented form only. Compare your implementation with the lowest-cost SOP implementation by giving the costs. 4M

2B. Write the two cases where correction has to be made during the addition of 2 BCD digits with examples. Write the Verilog code for a full adder. Using this module design the four bit adder. Using this four bit adder module write Verilog code for single digit BCD adder. 4M

2C. Using full adders design the simplest circuit that determines how many bits in a six-bit unsigned numbers are equal to 1. 2M

3A. A combinational circuit is specified by the following three boolean functions

F1(A,B,C) = ∑m(2, 4, 7) F2(A,B,C) = ∑m(0,3) F3(A,B,C) = ∏M(1,5,6)

Design the circuit using appropriate decoder and other gates. Write Verilog code to implement this design. Implement binary decoder module using case statement. 3M

3B. Using Shannon's expansion implement the following function using only 2:1 multiplexers. 3M

f = w1w2 + w2′w3 + w1w3

3C. Write the truth table for a 3 bit gray code to equivalent binary code. Design a 3 bit gray to binary converter using 2:1 multiplexers and other necessary gates. Write behavioral Verilog code to convert an N bit gray code into an equivalent binary code using for loop. 4M

4A. Draw the circuits for the Verilog code segments as given below in a) and b) using D Flipflops 2M

a)

```
always @ (negedge clock)
begin
   f = a|b ;
   g = f & ~(c^d);
   h = g ^ (a|d);
end
```

b)

```
always @ (negedge clock)
begin
    f <= a|b ;
    g <= f & ~(c^d);
    h <= g ^ (a|d);
end
```

4B. Design a synchronous counter with the following repeated binary sequence: 0, 1, 3, 7, 6, 4. Use T Flip-flops. Treat the unused states as don't care conditions. Analyze the final circuit to check if it is self-correcting or not. 5M

4C. Construct a JK Flip Flop using AND and NOR gates. Write the characteristic table of this flip flop considering all possible combinations of inputs and present state. What is the undesirable operation of the above construct? Mention the solutions used to overcome it. 3M

5A. Construct a 4 bit Johnson counter. Write the truth table showing the count sequence and AND gate expressions required for the output. 2M

5B. With a neat diagram explain the NMOS realization of AND gate. Consider the function

f = x1′ + (x2′ + x3′) x4′

Derive a CMOS circuit for this function by briefly explaining the required expressions. 4M

5C. i) Briefly explain four types of tri-state buffers with truth table and neat diagrams 2M

ii) Explain the functional structure of PLA with a gate level diagram 2M