III SEMESTER B.TECH (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: SWITCHING THEORY AND LOGIC DESIGN [CSE 203]

REVISED CREDIT SYSTEM
28-11-2015

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Obtain the simplest POS expression for f(a,b,c,d) = (a'+b+c) (a'+b'+d') (a'+c+d) Using algebraic manipulation and draw the circuit using only NOR gates. 2M

1B. Synthesize the minimum cost circuit using basic gates for the following function. Use algebraic manipulation for the simplification.Also write the truth table. 3M
f(a,b,c)=a'b'c'+a'bc'+a'bc.

1C. i. Define the following terms
a. Prime Implicant b. Cover of a logic function 2M
ii. Find the minimum cost SOP expression for the following function using K-map. f(a,b,c,d,e)= ∑m(0,2,4,6,9,13,21,23,25,29,31).Implement the minimal cost SOP expression using only NAND gates. 3M

2A. Simplify the function f(a,b,c,d)=∑m(6,7,8,9,10,11,14,15) using K-map and write all the prime implicants, essential prime implicants and the simplified expression 2M

2B. Use functional decomposition to find best implementation of the given function F=πM(1,2,3,5,6,7,9,10,11,12).Draw logic diagram for your implementation. Assume input variables are available in true form only. 2M

2C. i.Perform the following operations using 2's complement representation. Select enough bits to avoid overflow.
a. (+5) + (-2) b. (-7)-(-4) 2M
ii. Determine the minimum-cost SOP and POS expressions for the following function f(x1, x2, x3, x4) =∑m(4, 6, 8, 10, 11, 12, 15) + D(3, 5, 7, 9).Write the cost for each case. 4M

3A. Design a circuit to find the number of ones in a six bit unsigned number. 3M

3B. Design a single-digit BCD adder using four-bit adder and external gates. Write the VHDL code for the same using four-bit adder as a component. 4M

3C .i. Write the truth table and VHDL code for a full adder. 1M
ii. Design a 4 bit adder/subtractor circuit using full adders. 2M

4A. A combinational circuit is specified by the following Boolean function:

$F(A,B,C,D)= \Sigma(0,2,6,7,8)$

Use Shannon's expansion to derive an implementation using one 4:1 multiplexer and other necessary gates. Use A and B as selection inputs for the multiplexer 2M

4B. Design a 16:1 multiplexer using five 4:1 multiplexers. Write VHDL code for 4:1 multiplexer and using this as a component, write the VHDL code for 16:1 multiplexer using for generate statement 5M

4C. Write the truth table for 8 to 3 priority encoder and write behavioral VHDL code for the same using conditional signal assignment statement 3M

5A. Explain the operation of D-type positive edge triggered flipflop with suitable diagrams. 4M

5B. Design a sequential circuit with two D flip-flops, *A* and *B*, and one input, *x*. When $x = 0$,the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transitions from 00 to 01 to II to 10 back to 00, and repeats. 4M

5C. Draw the logic circuit and write characteristic table for the following

i. RS flipflop using NAND gates ii. T flipflop 2M

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6A. With a neat diagram, explain the working of CMOS NAND gate. 2M

6B. Design a counter with the following repeated binary sequence: 0, 4,7,2,3. Use JK flipflops. 4M

6C. i. List the possible states of a 4 bit ring counter. Also draw the sequence of timing signals generated by ring counter. 2M

ii. Differentiate synchronous and asynchronous counters. Draw the design of a 4-bit synchronous binary up counter using JK flipflop. 2M