Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKE UP EXAMINATIONS, DEC 2015 / JAN 2016

SUBJECT: ANALOG ELECTRONIC CIRCUITS [ELE 209]

REVISED CREDIT SYSTEM

Time: 3 Hours | 09 January 2016 | MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL** questions.
- Missing data may be suitable assumed.

1A. In the figure as shown in fig.Q1A, if Vi has a peak of 30 V, then draw the transfer characteristics. **4**

1B. In the figure as shown in fig.Q1B, identify the diode (V_D= 0.6 V) based circuit. **3**

1C. Design a Zener voltage regulator for the following specifications: output voltage = 5V, input voltage = 12 ± 3 V, load current = 20 mA, zener power rating = 500 mW. **3**

2A. Discuss the transconductance of MOSFET. Hence derive the equations governing the relationship between transconductance, current, aspect ratio and gate overdrive voltage of the MOSFET. **3**

2B. Assuming λ≠0, draw the small signal model of the circuit shown in Fig.Q2B. **3**

2C. Design the circuit shown in Fig. Q2C for a voltage gain of 5V/V and a power budget of 6mW. Assume that the voltage divider branch consumes 5% of total power and voltage drop across Rs is equal to the overdrive voltage of the transistor. Also assume R_D= 200Ω, V_{TH} = 0.4 V, μnCox = 200 μA/V2, λ=0. **4**

3A. For the NMOS common source amplifier shown in Fig. Q3A, the transistor parameters are: V_{th} = 0.8 V, $\mu_n C_{ox}$ (W/2L) = 1 mA/V^2, V_{DD} = 5V, R_s = 1 kΩ, R_D = 4 kΩ, R_1 = 225 kΩ, R_2 = 175 kΩ. Calculate the quiescent values I_{DQ} and V_{DSQ}. Draw the small signal model and hence determine the small signal gain for R_L is infinite. Neglect Channel length modulation. **5**

3B. Draw the BJT based voltage devider circuit and derive expression for stability of the ciruit. **5**

4A. Bandwidth of an amplifier lies between 150 Hz and 100 kHz. Find frequency range over which voltage gain is less than 2 dB from mid-band value. **3**

4B. Design an NMOS current mirror with V_{DD}=6V, V_{SS}=0V, I_{ref}=100μA. For the matched transistors L=10μm, W=100μm, V_{TH} =1V, $\mu_n C_{ox}$= 20μA/V^2. **3**

4C. For a class B Power amplifier providing a 20 V peak signal to a 8 Ω load (speaker) and a power supply of $V_{CC}=|V_{EE}|=30$ V, determine the input power, output power and efficiency of the circuit. **4**

5A. State and prove Millers theorem for a BJT based amplifier circuit and derive suitable expression for the gain of the circuit. **5**

5B. Derive the expression for conversion efficiency of Class A series fed and transformer coupled Power amplifiers. **5**

6A. Classify the power amplifiers based on angle of conduction. **2**

6B. Write a note on series and shunt voltage regulators. **4**

6C. Starting from 230 V, 50 Hz supply design a circuit to get an output of 5 V, 150 mA with ripple < 2%. **4**

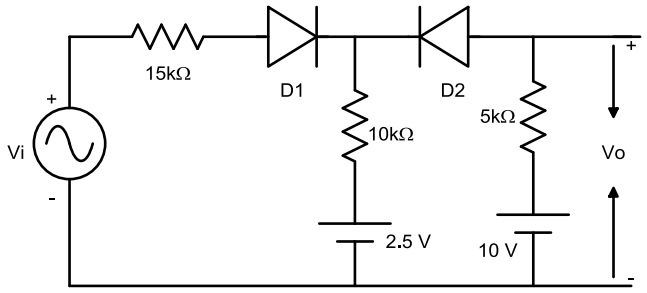

Fig Q1A

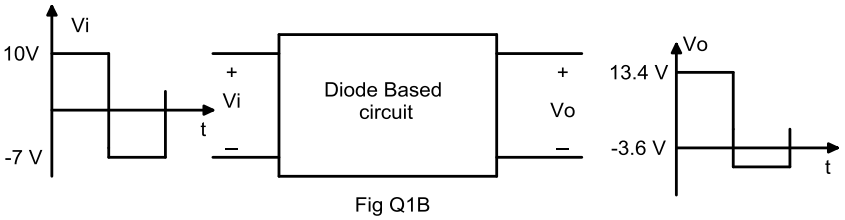

Fig Q1B

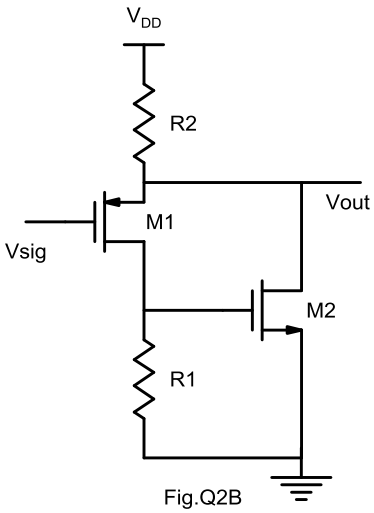

Fig.Q2B

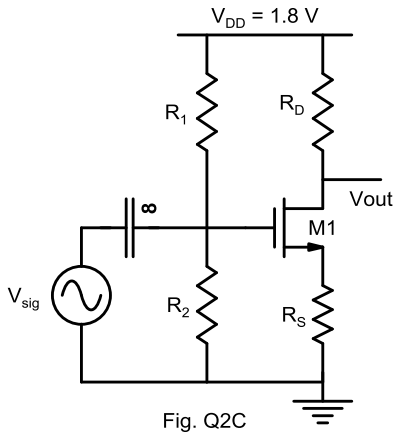

Fig. Q2C

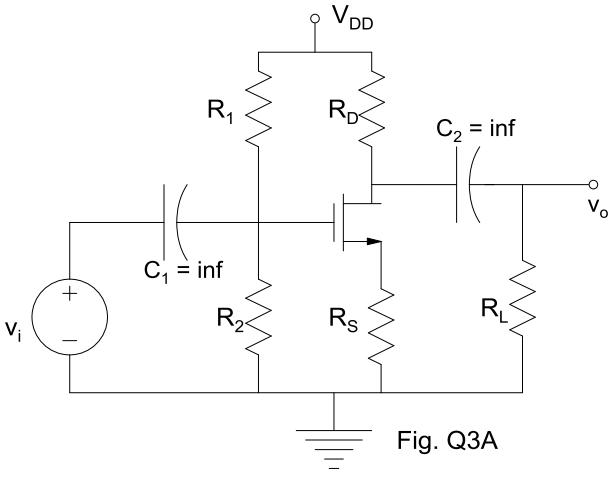

Fig. Q3A