Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: ANALOG ELECTRONIC CIRCUITS [ELE 209]

REVISED CREDIT SYSTEM

Time: 3 Hours 08 DECEMBER 2015 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE** Full questions.
- Missing data may be suitably assumed.

1A. Determine V_o, I, I_1 and I_2 for the circuit shown in Fig.Q1A. Assume Silicon diodes. **02**

1B. Plot v_o v/s time for the circuit shown in Fig. Q1B. Assume ideal diodes. **05**

1C. Parameters of a 6.3 V Zener diode for voltage regulator are: V_Z = 6.3 V at I_{ZT} = 40 mA and R_Z = 2 Ω. V_s varied between 12 V to 18 V. Minimum load current is 0mA. Minimum Zener diode current is 1 mA. Power dissipation of Zener diode must not exceed 750 mW at 25°C. Determine a) i_{zmax} b) value of R_s that limits the Zener current i_{zmax} to value determined in part a) and c) power rating of R_s. **03**

2A. Design a circuit to obtain the output voltage waveform shown in Fig. Q2A, for the given input waveform and justify. Assume silicon diodes. **03**

2B. Determine R_i, R_i', A_V, A_{Vs}, A_I and A_{Is} for the circuit shown in Fig.Q2B. Assume A_V to be very high. Draw the h parameter model. Given hie = 1.1 k, hfe = 50. **07**

3A. In the amplifier shown in Fig. Q3A, the MOSFET has V_{TH} = 0.7 V, μnCox = 500 μA/V2, λ = 0, drain current I_D = 1 mA. Determine

a) W/L and gm of the MOSFET
b) Maximum small signal gain from Vsig to Vo

03

3B. With a neat circuit diagram, discuss the MOSFET based RC coupled amplifier. Hence discuss the role played by each discrete circuit element in defining the gain and frequency response. **03**

3C. In the cascaded amplifier shown in Fig. Q3C, the MOSFETs have, drain currents I_{D1} = 2 mA, I_{D2} = 1 mA, V_{TH} = 0.7 V, $\mu_n C_{ox}$ = 500 μA/V^2, λ= 0

a) Draw the small signal model
b) Find the small signal gain from Vsig to V_L
c) Determine Rin and Rout of the amplifier.

04

4A. For the amplifier shown in fig. Q4A, if it is required to have cut-off frequencies as 1 kHz and 40kHz, then determine the values of capacitances C_1, C_2 and C_L. Assume λ = 0.01 per volt. **03**

4B. In the circuit shown in Fig Q4B, if $(\mu nCox)_1=(\mu nCox)_2$ = 200 $\mu A/V^2$, I_{D1} = 100μA, $V_{TH1}= V_{TH2}$= 0.4 V, λ = 0, $(W/L)_1$ = 5, then determine
a) Resistance R1
b) VDS2 if $(W/L)_2 = 0.1 \times (W/L)_1$ **03**

4C. With a neat circuit and diagram and necessary waveforms, evaluate maximum efficiency of a series fed class A power amplifier. Suggest suitable modifications to improve the efficiency. **04**

5A. Design a voltage divider bias circuit for following specifications: β= 50, V_{BE}= 0.7 V, V_{cc}= 22.5 V, R_c = 5.6 kΩ, Q point at V_{CE} = 12 V, I_C = 1.5 mA, S≤ 3. **03**

5B. For a class B Power amplifier providing a 20 V peak signal to a 8 Ω load (speaker) and a power supply of $V_{CC}=|V_{EE}|$=30 V, determine the input power, output power and efficiency of the circuit. **03**

5C. Write a note on Basic Series and Shunt Voltage Regulators with neat circuit diagrams. **04**

6A. For a full bridge rectifier supplying a load of 200 Ω from an ac source of 30 V at 50 Hz, calculate average load voltage and percentage ripple if a capacitor of 1000 μF is used as filter. **04**

6B. With relevant waveforms define storage time, transition time and reverse recovery time of PN junction diode. **03**

6C. Classify the power amplifier based on the conduction angle. **03**

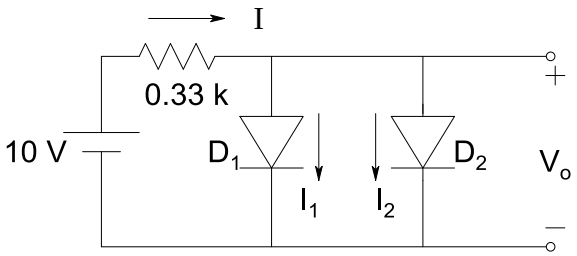

Fig.Q1A

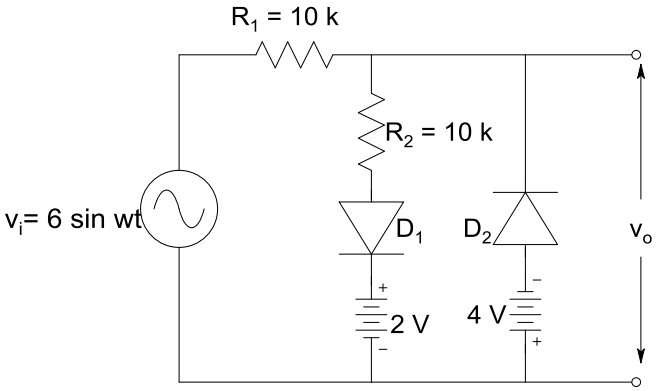

Fig. Q1B

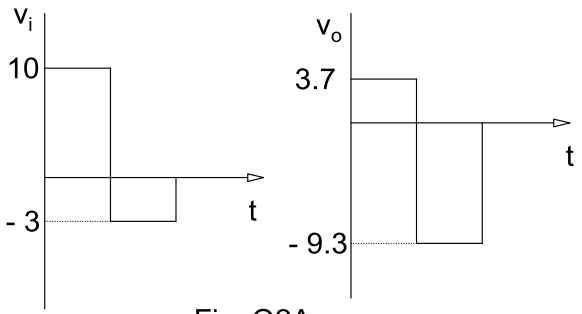

Fig. Q2A

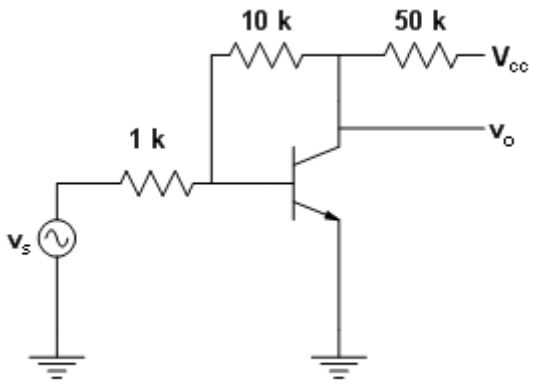

Fig.Q2B

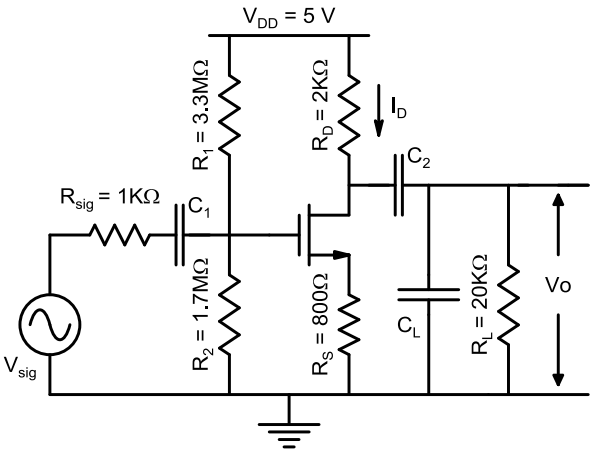

Fig. Q3A

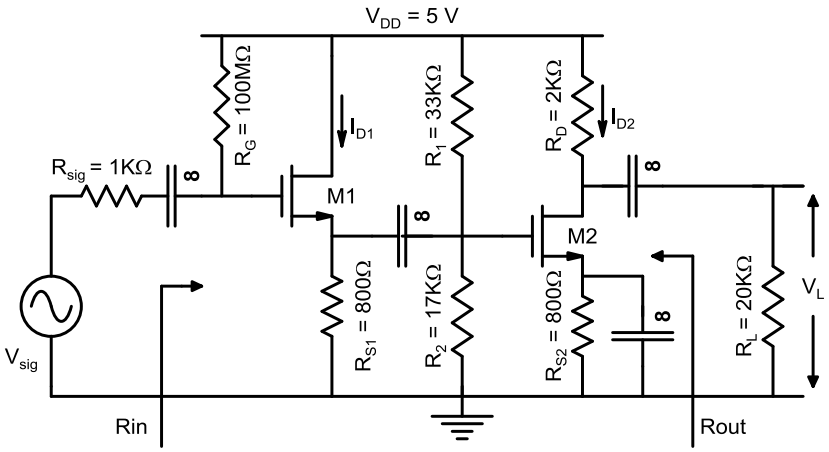

Fig. Q3C

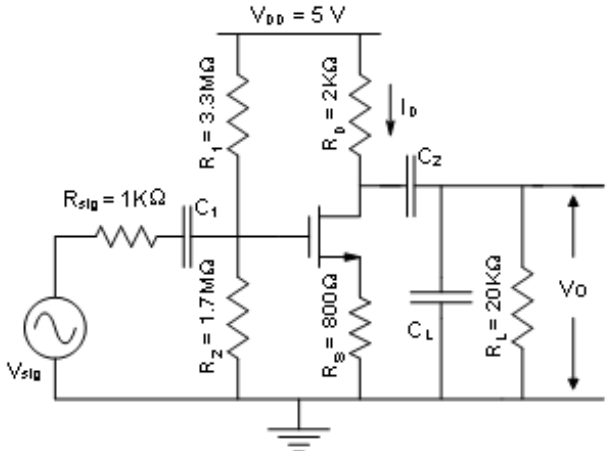

Fig.Q4A

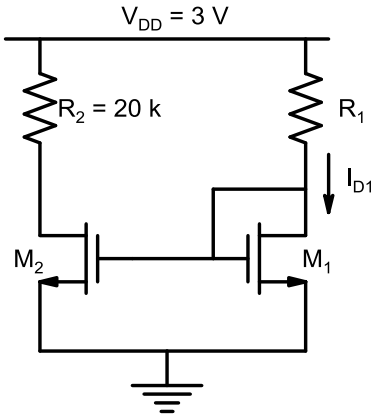

Fig. Q4B