Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: ANALOG ELECTRONIC CIRCUITS [ELE 2105]

REVISED CREDIT SYSTEM

Time: 3 Hours 08 DECEMBER 2015 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Determine V_o, I, I_1 and I_2 for the circuit shown in Fig.Q1A. Assume Silicon diodes. **02**

1B. Plot v_o v/s time for the circuit shown in Fig. Q1B. Assume ideal diodes. **05**

1C. Parameters of a 6.3 V Zener diode for voltage regulator are: V_Z = 6.3 V at I_{ZT} = 40 mA and R_Z = 2 Ω. V_s varied between 12 V to 18 V. Minimum load current is 0mA. Minimum Zener diode current is 1 mA. Power dissipation of Zener diode must not exceed 750 mW at 25°C. Determine a) i_{zmax} b) value of R_s that limits the Zener current i_{zmax} to value determined in part a) and c) power rating of R_s. **03**

2A. Design a circuit to obtain the output voltage waveform shown in Fig. Q2A, for the given input waveform and justify. Assume silicon diodes. **03**

2B. Using Miller theorem, determine voltage gain, input resistance and output resistance of MOSFET amplifier circuit shown in Fig. Q2B. Assume V_{th} = 1 V, $\mu_n C_{ox}(W/L)$ = 1 mA/V^2, λ = 0. Asume A_v to be large initially. Also draw the small signal model. **07**

3A. In the amplifier shown in Fig. Q3A, the MOSFET has V_{TH} = 0.7 V, μnCox = 500 μA/V2, λ = 0, drain current I_D = 1 mA. Determine

a) W/L and gm of the MOSFET

b) Maximum small signal gain from Vsig to Vo **03**

3B. With a neat circuit diagram, discuss the MOSFET based RC coupled amplifier. Hence discuss the role played by each discrete circuit element in defining the gain and frequency response. **03**

3C. In the cascaded amplifier shown in Fig. Q3C, the MOSFETs have, drain currents I_{D1} = 2 mA, I_{D2} = 1 mA, V_{TH} = 0.7 V, $\mu_n C_{ox}$ = 500 μA/V^2, λ= 0

a) Draw the small signal model

b) Find the small signal gain from Vsig to V_L

c) Determine Rin and Rout of the amplifier. **04**

4A. For the amplifier shown in fig. Q4A, if it is required to have cut-off frequencies as 1 kHz and 40kHz, then determine the values of capacitances C_1, C_2 and C_L. Assume $\lambda = 0.01$ per volt. **03**

4B. In the circuit shown in Fig Q4B, if $(\mu nCox)_1=(\mu nCox)_2 = 200\ \mu A/V^2$, $I_{D1} = 100\mu A$, $V_{TH1}= V_{TH2}= 0.4$ V, $\lambda = 0$, $(W/L)_1 = 5$, then determine

a) Resistance R1

b) VDS2 if $(W/L)_2 = 0.1 \times (W/L)_1$ **03**

4C. With a neat circuit and diagram and necessary waveforms, evaluate maximum efficiency of a series fed class A power amplifier. Suggest suitable modifications to improve the efficiency. **04**

5A. A MOS differential pair operated at a bias current of 1.8mA employs transistors with (W/L) of 100, $\mu_nC_{ox}=0.2mA/V^2$, $R_D=5k\Omega$ and $R_{SS}=20k\Omega$. Find the differential gain, common mode gain and the common mode rejection ratio if the output is taken single-endedly and the circuit is perfectly matched. **03**

5B. For a class B Power amplifier providing a 20 V peak signal to a 8 Ω load (speaker) and a power supply of $V_{DD}=|V_{SS}|=30$ V, determine the input power, output power and efficiency of the circuit. **03**

5C. Draw the circuit of an Active loaded MOS differential pair and discuss the merits of this circuit considering common mode and differential input voltage. **04**

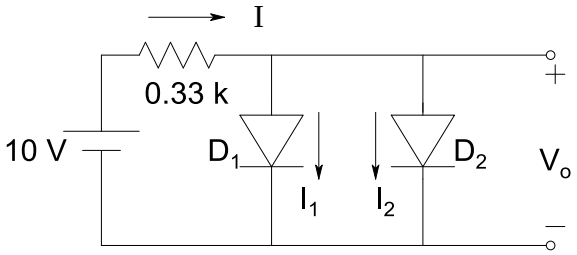

Fig.Q1A

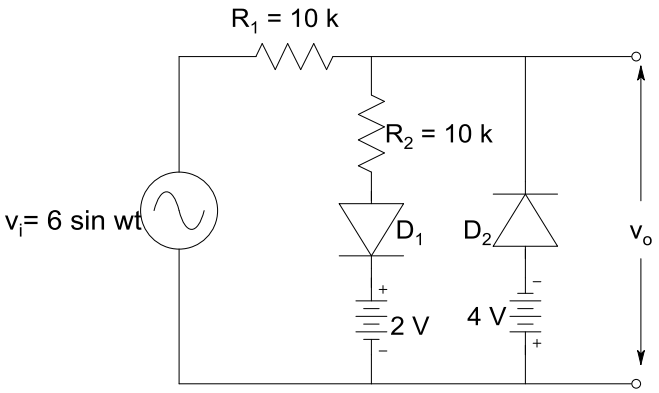

Fig. Q1B

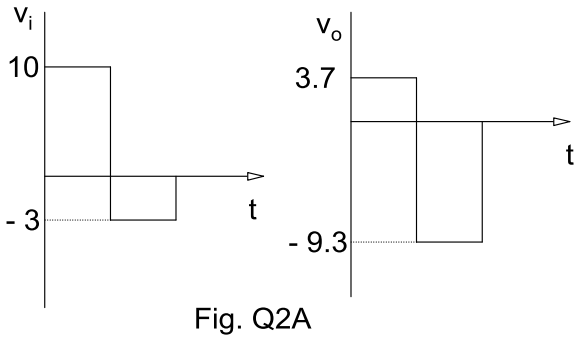

Fig. Q2A

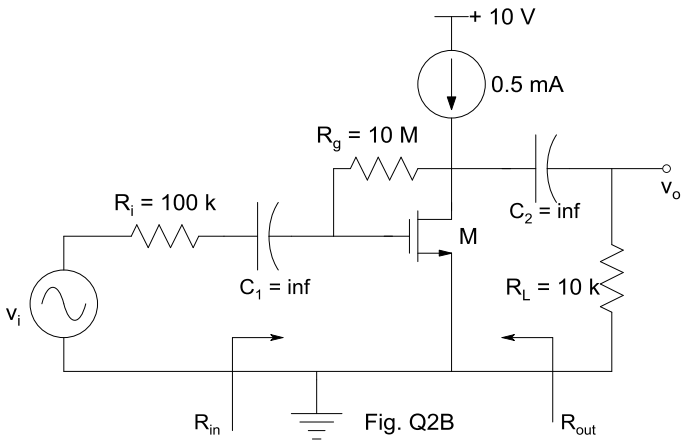

Fig. Q2B

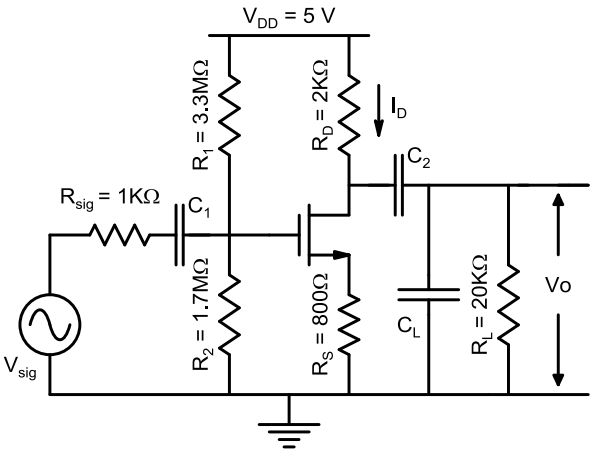

Fig. Q3A

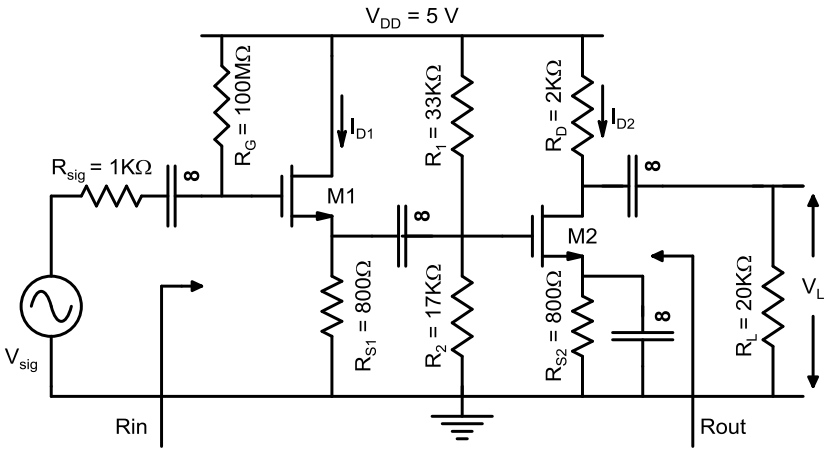

Fig. Q3C

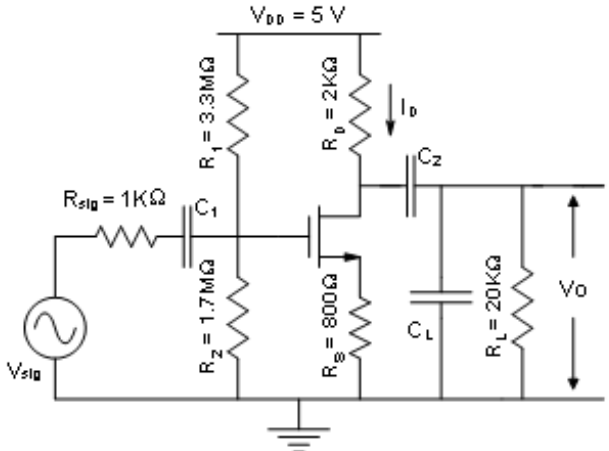

Fig.Q4A

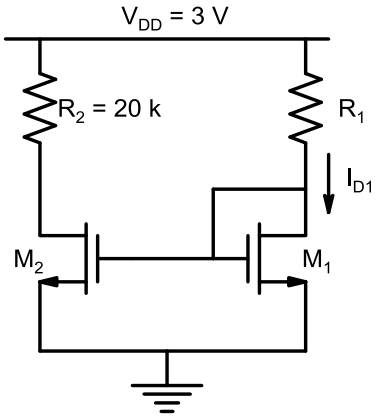

Fig. Q4B