Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ELE 2102]

REVISED CREDIT SYSTEM

Time: 3 Hours 01 DECEMBER 2015 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Given the network of Figure 1A , determine the functions f_2 and f_3 if $f_1 = \overline{A}$ and the overall function is to be
F(A,B,C,D)= $\Pi M(1,2,5,6,12,15) + d(3,4,8,10,13,14)$. Also Find G.

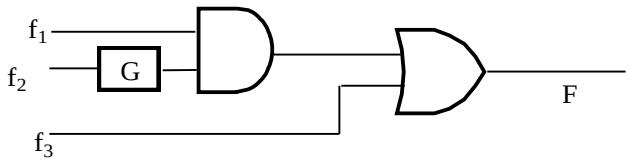

Figure 1A **(04)**

1B. Simplify the following Expression using VEM.
$F(A,B,C,D,E) = \prod M(0,1,7,8,9,12,14,18,19,21,27) + d(2,3,4,5,6,10,13,16,17,23,24,25,30,31)$ **(04)**

1C. A mux based circuit is given in the Figure 1C. Find the expression of Z0, Z1 and Z2.

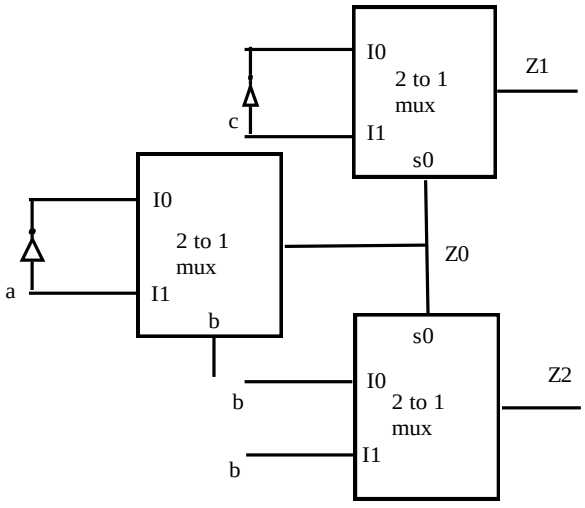

Figure 1C **(02)**

2A. Implement $f = a\bar{b} + \bar{a}c + bc$ using

1. Single 4:1 mux
2. 2 to 4 decoders **(04)**

2B. Design 2 digit BCD adder using 74LS283 **(04)**

2C. Draw the state diagram for the digital circuit shown in Figure 2C.

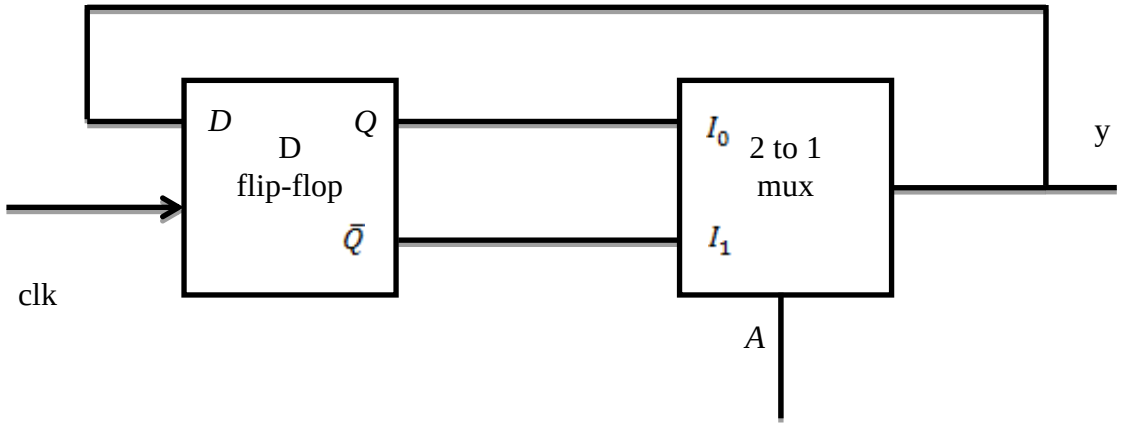

Figure 2C **(02)**

3A. Design a presettable counter which counts from 3 to 11 using D flip flops **(03)**

3B. Draw an ASM chart to detect the sequences 011 and 101 in a continuous data stream, as a Moore machine. **(04)**

3C. Design a 4 to 2 Priority encoder and mention its advantages. **(03)**

4A. Using a 4 bit universal shift register (74LS194) design a sequence generator which cycles through the following sequence. 0-8-12-6-13-11-7-3-1-0-….. **(04)**

4B. Design a two digit octal counter in the range 00-77 using 74LS90. **(03)**

4C. An AB FF is constructed from an SR FF as shown in Figure 4C

a) Obtain expression for S and R in terms of A and B.

b) Write an expression for the next state Q+ in terms of A, B and present state y.

c) Construct the excitation requirements table for A and B.

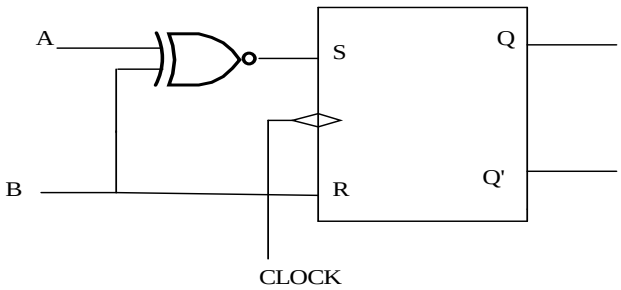

Figure 4C **(03)**

5A. A sequence Detector is to detect the sequence 1010 as a Mealy machine in a stream of 16 bits. Draw the state diagram and implement the circuit using D flip flops and 7493 IC. **(07)**

5B. Implement the equation $f = \bar{A} + A\bar{B}$ with CMOS logic. Use minimum number of MOS transistors. **(03)**