Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - 201)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A.	The circuit of Figure 1A is used to provide required phase shift in a oscillator. Show that $V'_f/V_o=1/(3+j(\omega RC-1/\omega RC))$. Also show that that the frequency of oscillation is $f=1/2\pi RC$ and the gain required for sustained oscillation is 3.
1B.	Calculate current gain, input and output resistance for the circuit shown in Figure 1B. Assume h_{ie} =1.1kΩ, h_{fe}=50, h_{oe}=25μ℧ and $h_{re}=2.5\times10^{-4}$.
1C.	i) Input characteristic of BJT can be used to determine ___ and ___ hybrid parameters ii) Out of fixed bias and self-bias circuits; we get stable operating point in case of ___
	(5+3+2)
2A.	Calculate Current gain, Voltage gain, input and output resistance for the circuit shown in Figure 2A. For the BJT, use h_{ie}=1kΩ, h_{fe}=50, h_{re} = h_{oe}=0.
2B.	In the hybrid-π model of BJT shown in Figure 2B, what does each component represent?
2C.	Given that. $\mathbf{V_{BE} = V + (R_b + R_e)\frac{\beta+1}{\beta} I_{C0} - \frac{R_b + R_e(1+\beta)}{\beta} I_C}$ Obtain an expression for stability factor $\boldsymbol{S = \frac{\partial I_C}{\partial I_{Co}}}$
	(5+3+2)
3A.	Determine the values of f_H, f_L and mid-band gain for the amplifier circuit shown in Figure 3A. Assume h_{ie}=1.1kΩ, h_{fe}=50, h_{re}= h_{oe}=0, $g_m=1.4\times10^{-3}$A/V, $r_{b'e}$=1kΩ, $c_{b'c}$=4pF, $c_{b'e}$=36pF.
3B.	Show that the transformer coupling has double the conversion efficiency over direct coupling?
3C.	A transistor supplies 0.85W of power to a 4kΩ load. The zero-signal dc collector current is 31mA, and the dc collector current with signal is 34mA. Determine the % of second harmonic distortion.
	(5+3+2)
4A.	Calculate voltage gain, input and output impedance for the FET amplifier shown in Figure 4A. Assume $g_m=2\times10^{-3}$A/V and r_d=40kΩ.
4B.	For an n-channel JFET obtain an expression for drain current I_D in terms of device parameters (a, w and L), electron mobility μ_n, doping concentration N_D, gate to source voltage V_{GS}, pinch-off voltage V_P and drain to source voltage V_{DS}.
4C.	In the circuit of Figure 4(C), i) we observe ___ and ___ configuration. ii) Q2 stage will have a current gain of less than one (T/F)
	(5+3+2)

5A.	In the circuit of Figure 5(A); BJT has h_{fe}=50, h_{ie}=1.1kΩ, h_{re}=h_{oe}=0; R_C=330Ω, R=47KΩ and R_E=120Ω. Determine the input resistance seen by the source V_i. Assume capacitor to act as short circuit at the operating frequency
5B.	Define three types of sweep error and derive a relation between them
5C.	i) Negative feedback _____ bandwidth and reduces _____ . ii) Current series feedback decreases ____, and increases _____, _____, and ____.
	(5+3+2)
6A.	Using necessary diagram and analysis of a sinusoidal oscillator using L and C; show that we need either two inductors and one capacitor or one capacitor and two inductors to construct a LC-oscillator. .
6B.	Verify if the following statements are True or False for the block diagram shown in Figure 6B. i) The block diagram represents Voltage shut feedback system ii) The type of feedback used here is useful in case of Current Amplifier iii) With feedback both the input and output resistance decreases.
6C.	Three identical cascaded stages have an overall upper 3-dB frequency of 20 kHz and lower 3-dB frequency of 20Hz. What are f_L and f_H of each stage? Assume non-interacting stages
	(5+3+2)

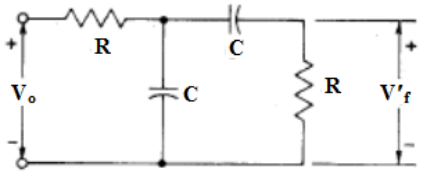

Figure 1A

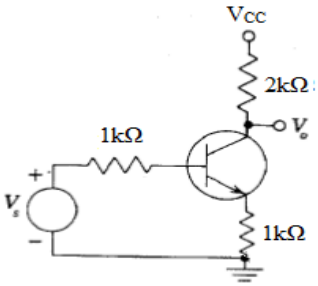

Figure 1B

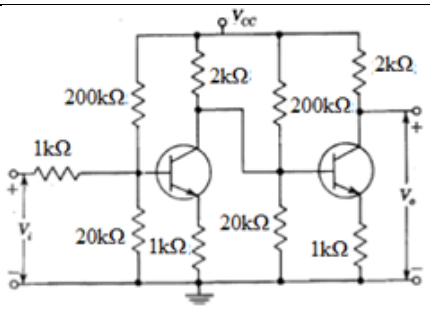

Figure 2A

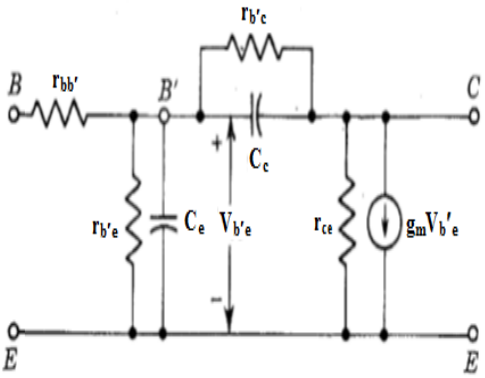

Figure 2B

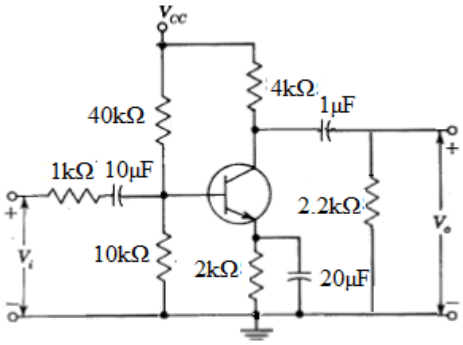

Figure 3A

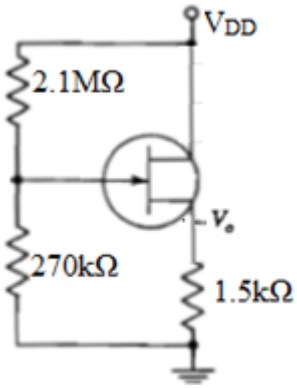

Figure 4A

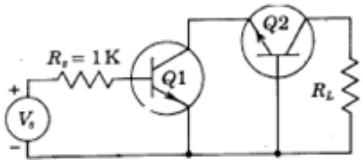

Figure 4C

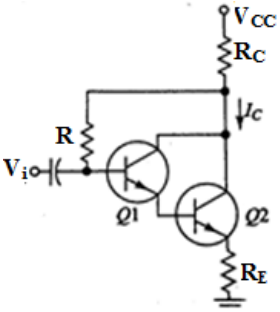

Figure 5A

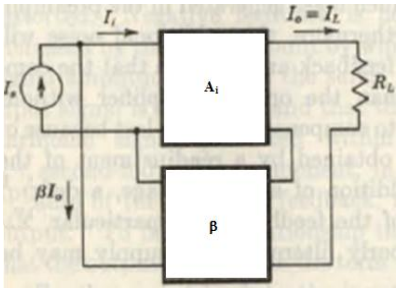

Figure 6B