Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - 2101)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Consider the circuit shown in Fig. Q1(A), where v_1 represents the signal generated by a microphone, $I_S=3\times10^{-16}$A, $\beta=100$, and Q_1 operates in the active mode. (i) If $v_1=0$, determine the small-signal parameters of Q_1. (ii) If the microphone generates a 1mV signal, how much change is observed in the collector and base currents?

1B. Due to a manufacturing error, the base width of a bipolar transistor has increased by a factor of two.

i) How does the collector current change?
ii) If this change has to be compensated by emitter area, what should be the emitter area with respect to original emitter area?
iii) If the transistor is a pnp transistor; is the current value same as that of npn transistor?

1C. A degenerated CE stage is biased at a collector current of 1 mA. If the circuit provides a voltage gain of 20 with no emitter degeneration and 10 with degeneration, calculate the value of R_C and R_E.

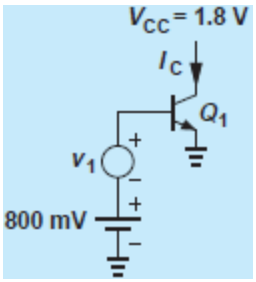

Fig. Q1(A)

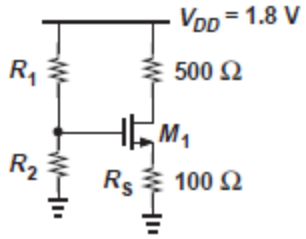

Fig. Q2(A)

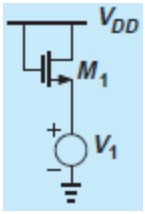

Fig. Q2(C)

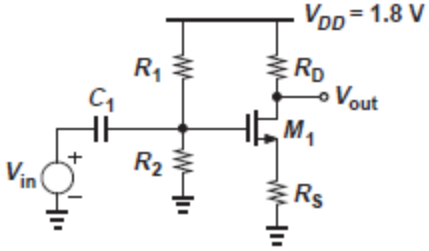

Fig. Q3(A)

(5+3+2)

2A. The circuit of Fig.Q2(A) must be designed for a voltage drop of 200mV across R_S. Assume $V_{TH}=0.4$V, $\lambda=0$ and $\mu_nC_{OX}=200\mu A/V^2$.
(i) Calculate the minimum allowable value of W/L if M_1 must remain in saturation.
(ii) Assuming $V_G=0.8$V, design the values of R_1 and R_2 to get the input impedance of at least 30kΩ.

2B. The drain current of an NMOS device is 1 mA with $V_{GS}-V_{TH}=0.6$V and 1.6mA with $V_{GS}-V_{TH}=0.8$V. If the device operates in the triode region, calculate V_{DS} and W/L. Assume $\mu_nC_{OX}=200\mu A/V^2$.

2C. Sketch the drain current of M_1 in Fig. Q2(C) versus V_1 , as V_1 varies from zero to V_{DD}. Assume $\lambda = 0$.

(5+3+2)

3A. Design the amplifier shown in Fig. Q3(A) to provide a voltage gain of 4 with a power budget of 2mW while the voltage drop across R_S is 200mV. The overdrive voltage of the transistor must not exceed 300mV and current through R_1 and R_2 is 5% of current drawn from supply. Assume V_{TH}=0.4V, and $\mu_n C_{OX}$=200μA/V^2.

3B. In the amplifier shown in Fig. Q3(B), collector current of Q_1 is 1mA, R_1=1kΩ & C_L=1pF. Calculate the frequency at which gain falls by 10%. Neglect the junction capacitors and channel length modulation.

3C. Figure Q3(C) is a two-stage amplifier consisting of a CS circuit and a source follower. Assuming λ≠0 for M_1 and M_2 but λ = 0 for M_3, and neglecting all capacitances except C_{GS3}, compute the output impedance of the amplifier.

(5+3+2)

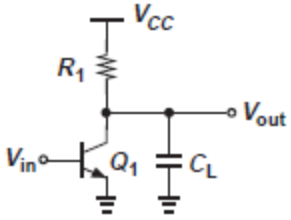

Fig. Q3(B)

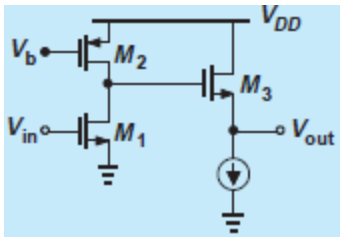

Fig. Q3(C)

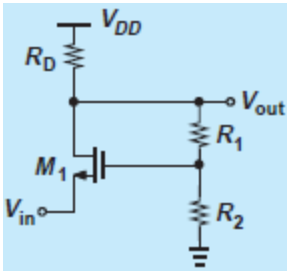

Fig. Q4(A)

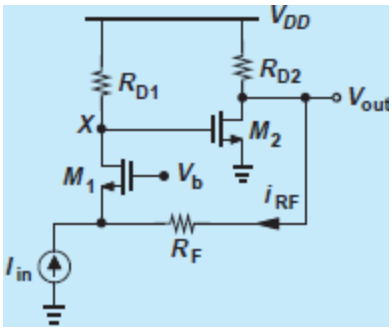

Fig. Q4(B)

4A. Calculate the closed loop gain, input and output resistance for the circuit in Fig. Q4(A).

4B. Identify the sense and return mechanisms, and the polarity of the feedback in the circuit of Fig. Q4(B). Redraw the circuit with no feedback.

4C. Calculate the loop gain of the circuit in Fig. Q4(C). Assume the Opamp exhibits an open-loop gain of A1, but is otherwise ideal. Also, λ = 0 for the MOSFET.

(5+3+2)

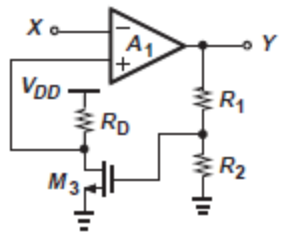

Fig. Q4(C)

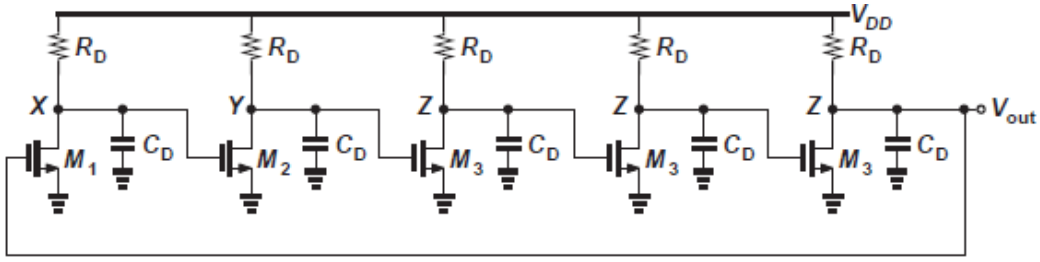

Fig. Q5(A)

5A. Derive the oscillation frequency and startup condition for the ring oscillator of Fig. Q5(A).

5B. For a BJT i_b=2μAcosωt and i_c=100i_b + 3i_b^2. Calculate the DC content in the collect current, amplitude of fundamental and 2nd harmonics. Also calculate the 2nd harmonic distortion in the collector current.

5C. Show that the transformer coupling has the best conversion efficiency of 50%.

(5+3+2)