Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - 2101)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design the circuit of Fig. Q1(A) for an input impedance of greater than 10kΩ and a g_m of at least 1/(260Ω). If β = 100, $I_S = 2\times10^{-17}$A, and $V_A = \infty$, determine the minimum allowable values of R_1 and R_2.

1B. In the circuit of Fig. Q1(B), if $I_{S1} = 2I_{S2} = 5\times10^{-16}$A, determine V_B such that I_X = 1.2mA.

1C. (i) Calculate the output voltage for the circuit shown in Fig. Q1(Ci). Assume $I_S = 5\times10^{-16}$A.
(ii) A BJT carries a collector current of 1 mA with V_{CE} = 2V. If V_A = 20V and $I_S = 2\times10^{-16}$A, calculate the value of V_{BE}.

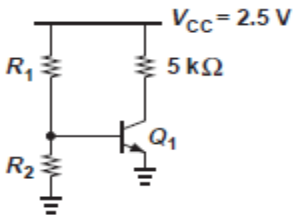

Fig. Q1(A)

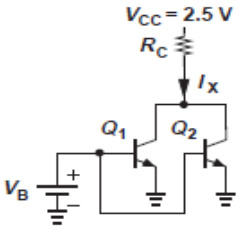

Fig. Q1(B)

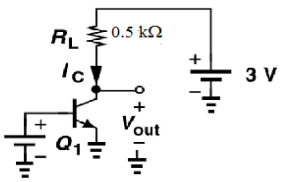

Fig. Q1(Ci)

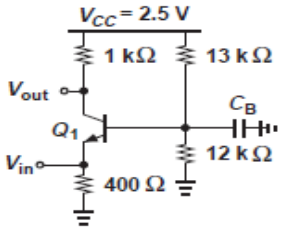

Fig. Q2(A)

(5+3+2)

2A. The CB stage in Fig. Q2(A) has β = 100, $I_S = 8\times10^{-16}$A, $V_A = \infty$, and C_B is very large. (i) Determine the operating point of Q_1. (ii) Calculate the voltage gain and I/O impedances of the circuit.

2B. An NMOS device operating in saturation has $\mu_n C_{OX}$=200μA/V^2 and λ=0 and it must provide a transconductance of 1/(50Ω).
(i) Determine W/L if I_D = 0.5 mA.
(ii) Determine W/L if $V_{GS} - V_{TH}$ = 0.5V.
(iii) Determine I_D if $V_{GS} - V_{TH}$ = 0.5V.

2C. If V_{TH} = 0.4V, determine the region of operation of M_1 in each of the circuits shown in Fig. Q2(C).

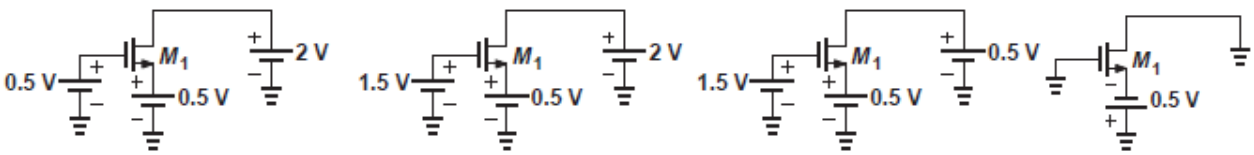

Fig. Q2(C)

(5+3+2)

3A. Design the circuit of Fig. Q3(A) for a drain current of 1 mA. If W/L = 20/0.18, compute R_1 and R_2 such that the input impedance is at least 20 kΩ. Assume $\mu_n C_{OX}$=200μA/V^2, λ=0 and V_{TH} = 0.4V.

3B. Using Miller's theorem to obtain an expression for the input and output poles of the circuit shown in Fig. Q3(B). Assume $V_A = \infty$ and neglect all other capacitances.

3C. For the circuit shown in Fig. Q3(C) determine $(W/L)_2$ for a voltage gain of 3. Assume $(W/L)_1$ = 20/0.18 and λ = 0. Derive the formula used.

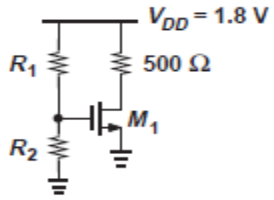

Fig. Q3(A)

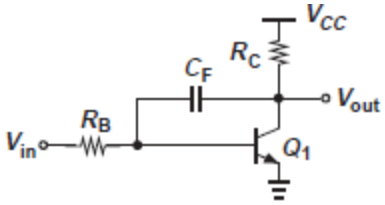

Fig. Q3(B)

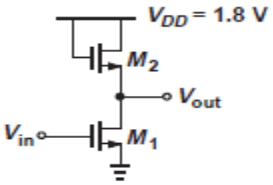

Fig. Q3(C)

(5+3+2)

4A. Design the transimpedance amplifier of Fig. Q4(A) for a closed loop gain of 1kΩ. Assume each transistor carries a collector bias current of 1 mA, β = 100, $V_A = \infty$, and R_F is very large.
(a) Determine the values of R_C and R_M for an open-loop gain of 20kΩ and an open-loop output impedance of 500Ω. (b) Compute the required value of R_F. (c) Calculate the closed-loop I/O impedances.

4B. Identify the sense and return mechanisms, and the polarity of the feedback in the circuits of Fig. Q4(B1) and (B2).

4C. Estimate the input capacitance of the source follower shown in Fig. Q4(C). Assume λ≠0.

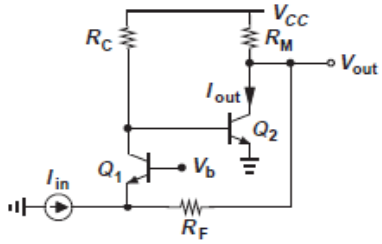

Fig. Q4(A)

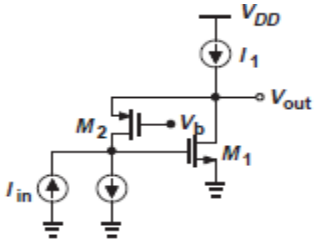

Fig. Q4(B1)

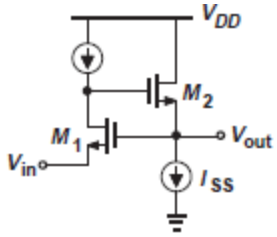

Fig. Q4(B2)

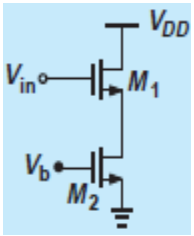

Fig. Q4(C)

(5+3+2)

5A. For the oscillator circuit in Fig. Q5(A), obtain an expression for frequency of oscillation. Determine the start-up condition for the oscillations.

5B. Show that a Class B Amplifier has a maximum conversion efficiency of 78.5.

5C. For the push-pull stage of Fig. 5(C), sketch the base current of Q_1 as a function of V_{in}.

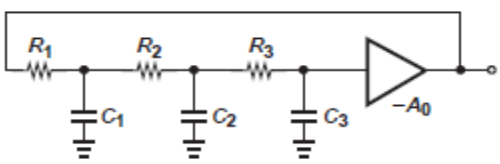

Fig. Q5(A)

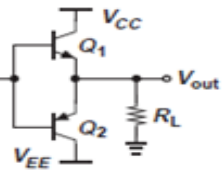

Fig. Q5(C)

(5+3+2)