Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 207)
TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Write the different instruction types by giving suitable example for each.
1B. Draw the hardware for based and stack based machine. Show the stack operation for the expression given below: y=((A+B)- (C+D))/E
1C. For the expression given below write three address and two address instructions using register. Y= (A*B+ C-D) / (E+F)

(5+3+2)

2A. Design a 4 stage carry look ahead adder and compute the total delay.
2B. Build hardware to implement each of the following register transfers:
i)If X is odd then A←B+C else A←B-C ii) If A=0 and D[1]=1 then A←B Assume A, B,C,D are 4 bit registers.
2C. Given full adder time 2ms and clock frequency 1KHz, calculate the time required to complete the add operation for a 8, 3bit operand in Series parallel approach.

(5+3+2)

3A. Design a 4 bit combinational shift register for the following:

Selection inputs		Clock input	Clear input	Operation
S1	S0	CLK	CLR	
0	0	H	L	No operation
0	1	H	L	Logical shift right
1	0	H	L	Arithmetic shift right
1	1	H	L	Rotate right

3B. Multiply - 6 x 9 using Booth's multiplier. Show all the iterations.
3C. Compare interrupt IO with conditional programmed IO?

(5+3+2)

4A. Starting from the state diagram, make a PLA implementation for a Booth's multiplier controller.
4B. Draw the 3 stage instruction pipeline diagram and explain. Write the different pipeline hazards by giving suitable example.
4C. Convert the IEEE floating-Point number 4351D000 H into equivalent decimal floating point number.

(5+3+2)

5A. Explain the DMA operation with a neat diagram. Discuss how DMA can improve the performance of a computer.
5B. Calculate the average memory access time Ŧ , the ratio of main memory access time to cache access

time γ, and efficiency Λ. Given that cache memory access time t_c= 160ns, main memory access time t_m=960ns and hit ratio h =0.9.

5C. What is op-code encoding? Give the various encoding techniques. Which method is optimum?

(5+3+2)

6A. Design a 4 bit, 8 function arithmetic unit that will meet the following specifications.

S0	S1	S2	F
0	0	0	2A
0	0	1	A+B’
0	1	0	A+B
0	1	1	A-1
1	0	0	2A+1
1	0	1	A+B’+1
1	1	0	A+B+1
1	1	1	A

6B. Write a Wallace tree structure for 6 operand summation. Give the expression for delay computation and compute the delay for the above Wallace structure.

6C. With suitable example, explain the following addressing modes: i) indirect ii) indexed.

(5+3+2)