Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 207)
TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. In a computer instruction format, the instruction length and size of the address field are 11 and 4 bits respectively. The instruction set has 6 two address and 24 zero address instructions. Using expanding op-code technique, compute the number of one address instructions that can be added to the instruction set.

1B. Draw the hardware of general register based, accumulator based and stack based machines.

1C. For the expression given below write two address and one address instructions without using any register. Y= (A*B+ C-D) / (E+F)

(5+3+2)

2A. Design an ALU for the following function:

S_2 S_1 S_0	Output
000	A+B
001	A-B
010	2A
011	A+1
100	A AND B
101	A OR B
110	A XOR B
111	0

2B. Multiply - 4 x 7 using Booth's multiplier. Show all the iterations.

2C. What is DMA ? Write the various handshake signals used in DMA process.

(5+3+2)

3A. Using 4 X 4 Combinational shifter as a basic block, design a Combinational shifter capable of rotating 16 bit data to the left by 0, 1, 2 or 3 bit.

3B. Draw the block diagram representation of polled and daisy chain interrupt.

3C. Build hardware to implement each of the following register transfers:

i)If X is even then A←B+C else A←B-C ii) If C=B and D[1]=1 then A←B Assume A,B,C,D and X are 4 bit registers.

(5+3+2)

4A. Draw the flowchart of non- restoring division algorithm.

4B. The parameters of a computer memory system having main memory size= 8K blocks, cache meory size=512 blocks and block size =8 words. Determine the size of the tag field of the main memory under the following conditions: a) Fully associative mapping b) Direct mapping.

4C. Illustrate the following addressing modes:

i) Indirct ii) Implicit

(5+3+2)

5A. Design the processing section of the Booth's multiplier. Show the various control signals used and define them.

5B. Write the 4 bit general register and give the truth table controlling the operation of the general register.

5C. Draw the five stage instruction pipeline diagram. Mention the pipeline hazards.

(5+3+2)

6A. Write the different instruction types by giving suitable example for each.

6B. Compare standard I/O with memory mapped I/O. Give the relevant instructions used in the same.

6C. Convert the IEEE floating-Point number 4351D000 H into equivalent decimal floating point number.

(5+3+2)