Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: LOGIC DESIGN (ECE - 205)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Given f(a,b,c,d) = ∑m(0,1,4,6,7,9,11,13,15)+∑d(2,3,10,12). Simplify the expression using K-map and answer the following questions.
   a) The reduced expression has ….minterms with ……variables each.
   b) Realizing the reduced expression using 2 input AND gates; two input OR gates and NOT gates requires ….AND gates, …OR gates and …..NOT gates.
   c) There are ….essential prime implicants.
   d) The reduced expression can also be realized using ….two input AND gate/s, …..two input OR gate/s , ….two input XOR gate/s and ….NOT gate/s.
   e) In the reduced expression every minterm contains variable…

1B. Using positive edge triggered J-K flip-flops design a suitable circuit that will give an output clock with 1/16 of input clock frequency. Draw the relevant waveforms.

1C. Implement the following function using a 8:1 MUX using a,b and c as select inputs.
F(a,b,c,d) = ∑m(1,2,4,5,7,9,11,12).

(5+3+2)

2A. Consider the decoder circuit diagram shown in FIGURE 2A. Plot 'y' considering all possible combinations of the inputs a, b and c.

2B. The working of a clocked MN flip-flop is as follows – when both M and N are low the flip-flop output sets, when M is low the flip-flop output doesn't change, when M input is high the flip-flop output toggles and when both M and N are high the flip-flop resets. Obtain the flip-flop using a JK flip-flop.

2C. Draw the state diagram and write the state table for a Mealy type serial binary adder

(5+3+2)

3A. Simplify the following Boolean expression using i) Quine Mc-Cluskey method ii) VEM with 'z' as the map entered variable. $F(w,x,y,z) = \bar{x}\bar{y}\bar{z} + \bar{w}xz + \bar{w}xy\bar{z} + \bar{w}xyz$.

3B. Draw the ASM chart for a full subtractor.

3C. Write the flow table for an asynchronous sequential circuit with 2 inputs X and Y and one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, output does not change for any change in X.

(5+3+2)

4A. Design a synchronous counter to count the sequence 0,2,4,6,1,3,5,7 and repeat. Use a flip-flop having the truth table given in TABLE 4A.

4B. Design a single digit BCD adder using 4 bit binary adder block

4C. Given that $(292)_{10} = (1204)_b$. Determine the base 'b'.

(5+3+2)

5A. Design an asynchronous sequential circuit to perform the following task. Switch ON a water pump when the water level goes below a level X_1 and keeps it ON till the water level goes below X_2. Pump is switched OFF when the water level exceeds X_2 and it remains OFF till water level goes below X_1. Note that X_i goes high when the water level goes above it and goes low when the water level goes below it.

5B. Define the following: (1) Fan out (2) Noise Margin (3) Propagation delay

5C. The message below has been encoded using even parity Hamming code and assumed to be received with single bit error. Determine the transmitted message.
10000111101001000000000101011.

(5+3+2)

6A. Design a Mealy type non-overlapping sequence detector using D flip-flops to detect the presence of the sequence 1010 and 1100.

6B. Simplify the following Boolean expression and implement the simplified expression using NAND gates. $F(A,B,C,D) = AB + A\overline{B}C + B\overline{C}$

6C. Starting from MSB, a binary number 10111011 is fed to a 8 bit SIPO with data entering from left. The initial content of shift register is assumed to be 10101010. What will be the shift register output at the end of 2 clock pulses and at the end of 8 clock pulses?

(5+3+2)

TABLE 4A

A	B	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	$\overline{Q_n}$

FIGURE 2A