Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: LOGIC DESIGN (ECE - 205)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Design Excess-3 to 8421 code converter using active low 4 to 16 decoder.

1B. Convert the following flip-flops.

a) SR to JK flip-flop
b)D to T flip-flop

1C. Draw the circuit diagram and write the counting sequence of a 4 bit ring counter.

(5+3+2)

2A. Design a synchronous counter using D flip-flops to count the sequence 0,1,2,5,7 and repeat.

2B. Encode each of the BCD digits using the weighted codes (i) 6 3 1 -1 (ii) 7 3 2 -1. Determine which of the codes is self-complementing.

2C. Find the minimal product(POS) expression for the function;

$F(a,b,c,d)=\sum m(0,1,2,3,4,6,9,12,14)+d(5,7,15)$

(5+3+2)

3A. Write Excitation table, Transition Table, State table, Flow table and Flow diagram for the following asynchronous sequential circuit which has two inputs x, y, two SR flip-flops and one output Z.

$S_1 = x\overline{Q}_2$

$R_1 = xQ_2$

$S_2 = xyQ_1$

$R_2 = \overline{x}\,\overline{y} + \overline{x}\,\overline{Q}_1$

$Z = x\overline{Q}_2 + Q_1\overline{Q}_2$

3B. Find minimal sum(SOP) expression for the function $F(w,x,y,z)=\sum m(0,5,6,7,9,13,14,15)$ using Quine Mc-Cluskey method.

3C. Implement a full subtractor using a 4:1 MUX

(5+3+2)

4A. Design a logic circuit that has a 4 bit binary number as an input and one output. The circuit outputs a '1' when the input is a prime number. Implement the circuit using NAND gates.

4B. Prove the following Boolean expressions:

$$a)(B+BC)(B+\overline{B}C)(B+D)=B$$
$$b)A\overline{B}C+B+B\overline{D}+AB\overline{D}+\overline{A}C=B+C$$

4C. Simplify the Boolean expression and implement using NOR gates

(5+3+2)

5A. Design a Mealy type sequence detector using T flip-flops to detect an overlapping sequence 1010.

5B. Design a positive edge triggered asynchronous decade counter.

5C. A n bit shift register is fed with a n bit data. Write the number of clock pulses required to shift n bit data out of the shift register if it is a (i) SISO (ii) PISO shift register.

(5+3+2)

6A. Design a 16 bit carry look ahead adder using 4 bit CLA adder blocks.

6B. Draw the ASM chart for a mod-6 up-down counter

6C. Synchronous counters are faster than Asynchronous counters. Give reasons

(5+3+2)