Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: LOGIC DESIGN (ECE -2105)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Using Tabular method, Obtain the minimal expression for f=∑m(0,1,3,7,8,12) + d (5,10,13,14)
1B. Design BCD adder using suitable circuit
1C. Briefly explain the terms i) Noise margin and ii) Propagation delay as applicable to logic gates.

(5+3+2)

2A. Simplify the following expression using K-map and implement it using minimum number of NOR gates. F= ∑m(6,9,13,18,19,25,27,29,31)+d(2,3,11,15,17,24,28)
2B. Implement full substractor using decoder logic. Assume active high inputs and active low outputs.
2C. For the given binary data 1010 obtain i) gray code ii) 7 bit Hamming code

(5+3+2)

3A. Design a synchronous counter using D flip-flops that goes through the state 1, 3, 5, 6, ….. Design the counter such that whenever it enters invalid state it needs to go back to the state 1.
3B. Reduse the following using 3 variable A,B,C using VEM method
F= A'B'C' + A'B'CD + A'BDE' + A'BC'E + AB'C + ABC + ABC'D'
3C. Implement f(x,y,z) = ∑(0,2,3,5) using 4:1 MUX with x,z as select lines

(5+3+2)

4A. Design a 1101 overlapping sequence detector using Melay model with JK flipflops
4B. Explain the working of master slave JK flip-flop with circuit diagram.
4C. Draw the ASM chart for synchronous 3 bit up-counter.

(5+3+2)

5A. Design a fundamental mode asynchronous sequential machine, which has two inputs x_1, x_2 and one output z. The output z = 1 only when $x_1 = x_2 = 1$ and x_2 becomes 1 before x_1. Draw the state table, minimize and design the machine. Show all the design steps.

5B. Design a 4 bit Universal Shift register circuit that performs shifting as per the following table.

S1	S0	Operation
0	0	No Change
0	1	Shift Right
1	0	Shift left
1	1	Parallel load

5C. Consider P-Q flipflop with two inputs P,Q and output R. If both inputs are '0', the output toggles, when both inputs are '1', then no change in input, When PQ="01" output is '1' and when PQ="10" output is '0'. Convert P-Q flip flop to D flip flop.

(5+3+2)