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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

**THIRD SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION**
**NOV/DEC 2015**
**SUBJECT: LOGIC DESIGN (ECE -2105)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. For the given Binary number $B_3B_2B_1B_0$, find its equivalent gray code $G_3G_2G_1G_0$. Note that $B_3$ and $G_3$ are MSBs. Implement $G_3$ using basic gates, $G_2$ using 3:8 decoders, $G_1$ using 8:1 MUX, $G_0$ using 4x4x2 PAL.

1B. Simplify the following Boolean expression using Quine Mc-Cluskey method. $F(A,B,C,D) = \sum m(1,2,3,5,9,12,14,15)+\sum d(4,8,11)$.

1C. Given $F(A,B,C,D,E)= \prod M(0,1,4,5,10,11,26,27)$. Find the minimal product and implement using NOR gates.

(5+3+2)

2A. Design a 4 bit multiplier which multiplies $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$ using half adders, full adders and AND gates only.

2B. Design a 3 bit odd parity generator and corresponding checker using 4:1 MUXes.

2C. Plot the transfer characteristics of a transistor TTL inverter and indicate the IC parameters

(5+3+2)

3A. Design synchronous overlapping sequence detector which will detect "010" and "101" sequence in a binary input stream using D flip-flops

3B. Design synchronous mod 6 down counter using T flip-flops.

3C. Write the truth table and transition table for the circuit shown in Fig.3C

(5+3+2)

4A. Design a fundamental mode asynchronous sequential circuit using D latch satisfying following conditions-

(i) A water tank has two sensors $X_1$ and $X_2$. The sensor $X_1$ is kept at lower level of the tank and $X_2$ at the top level of the tank.

(ii) The system has one output S which will become high when water level in the tank goes below $X_1$ and it will remain high till water level reaches X2.

4B. Design a bidirectional 3 bit shift register using D flip-flop and 2:1 Mux.

4C. Draw ASM chart for a 3 bit synchronous up-down counter.

(5+3+2)

5A. Write excitation table, next state table, state table and state diagram for the following synchronous sequential circuit. $J_1=X$ $K_1=YQ_2$ $J_2=X+Q_1$ $K_2=Y$ $Z_1=Q_1Q_2$ $Z_2=Q_1+Q_2$

Where $X_1,X_2$ are inputs, $Z_1,Z_2$ are outputs and $Q_1,Q_2$ are flip-flop outputs

5B. (i) Convert SR flip-flop to JK flip-flop

(ii) Convert D flip-flop to T flip-flop

5C. Design ripple decade up counter using negative edge triggered JK flip-flops

(5+3+2)

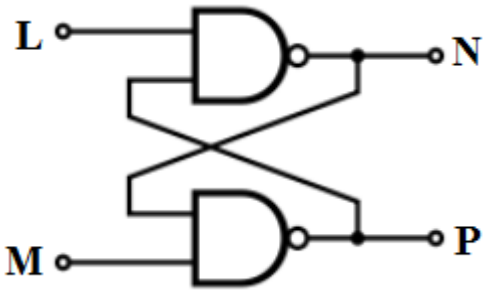


Fig. 3C