Reg. No.										

प्रज्ञानं ब्रह्म

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MANIPAL INSTITUTE OF TECHNOLOGY, MANIPAL 576104

(Constituent College of Manipal University)

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THIRD SEMESTER B. TECH. (IT) DEGREE MAKE UP EXAMINATION, JAN – 2016
SUBJECT: DIGITAL SYSTEMS – ICT 2102
(REVISED CREDIT SYSTEM)

TIME: 3 HOURS **01/01/2016** **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data, if any, may be suitably assumed.

1A. Design a sequence detector with one input Y and one output Z using Moore model. The output Z is HIGH whenever the sequence "110101" is detected, otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using D- flip flops and minimum external gates.

1B. Using 74138 IC and external NAND gates, design the combinational circuit to implement following functions:

$F_1(A, B, C) = \overline{A} + A\overline{C}$

$F_2(A, B, C) = \overline{A} + BC$

$F_3(A, B, C) = A\overline{B} + \overline{A}B$

1C. Design a 4-bit bi-direction shift register using JK-flip flops and external gates.

[5+3+2]

2A. Design a code converter to convert a decimal digit represented in Excess-3 to decimal digit represented in 8 4 -2 -1 code, using NAND gates only.

2B. What is Race around condition in JK – Flip Flop? With necessary diagrams, explain how master–slave JK – flip flop overcomes the same.

2C. Represent the following logic expression in canonical forms. $f = \overline{a}b + \overline{b} + a(c + b)$

[5+3+2]

3A. Simplify the given function 'F' using tabulation method. Implement the simplified expression using NAND gates only. $F(A, B, C, D, E) = \sum_m(0,1,3,5,6,9,11,12,15,27) + \sum_d(2,8,21,22,30)$

3B. Design a 32: 1 MUX using 4: 1 MUXs ONLY.

3C. Design MOD – 8 Johnson counter using D – flip flops. Write the counting sequence.

[5+3+2]

4A. Design a self starting synchronous counter using JK – flip flops and external gates to count the sequence 1 → 3 → 6 → 9 → 12 → 5 →1.

4B. Implement the following logic functions using suitable PLA $f_1 = \sum_m(0,4,5,7)$ $f_2 = \prod_M(1,2,4,5)$

4C. Design a logic circuit which divides the frequency of the input square wave by a factor of '12' while producing an output waveform with 50 percent duty cycle.

[5+3+2]

5A. Using 74193 ICs, 7485 ICs and minimum number of external gates, design an 8-bit binary down counter to count from N1 to N2 where N1 > N2.

5B. Give an asynchronous sequence generator circuit, using positive edge triggered JK – flip flops, to generate a sequence 1 0 1 0 0 0. Use external gates if required.

5C. Design 1 – bit magnitude comparator with cascading inputs using NOR gates only.

[5+3+2]