Reg. No.										

प्रज्ञानं ब्रह्म

Manipal
INSPIRED BY LIFE

MANIPAL INSTITUTE OF TECHNOLOGY, MANIPAL 576104

(Constituent College of Manipal University)

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MANIPAL INSTITUTE OF TECHNOLOGY

THIRD SEMESTER B. TECH. (IT) DEGREE END SEMESTER EXAMINATION, NOV/DEC – 2015
SUBJECT: DIGITAL SYSTEMS – ICT 2102/ ICT 203
(REVISED CREDIT SYSTEM)

TIME: 3 HOURS **28/11/2015** **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data, if any, may be suitably assumed.

1A. Simplify the given function 'F' using tabulation method. Implement the simplified expression using NOR gates only. $F(v,w,x,y,z) = \prod_{M}(2,4,6,7,9,11,14,19,27,30,31) \bullet \prod_{D}(5,15,29)$

1B. Convert a given D – flip flop to work as JK – flip flop.

1C. Design a full subtractor using two half subtractors and one OR gate.

[5+3+2]

2A. Design a sequence detector with one input X and one output Y using Mealy model. The output Y is HIGH whenever the sequence "010110" is detected. Otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using T- flip flops and minimum number of external gates.

2B. Design 2 – bit magnitude comparator using a suitable ROM.

2C. For a MOD – 6 Johnson counter show that decoding can be done using 2 – input AND gates only.

[5+3+2]

3A. Using 7493 ICs, 7485 ICs and minimum number of external gates, design a 2-digit BCD up counter to count from 0 to N.

3B. Give an asynchronous sequence generator circuit, using negative edge triggered SR – flip flops, to generate a sequence 1 1 1 0 0 0. Use external gates if required.

3C. Design 4 to 2 priority encoder using basic gates.

[5+3+2]

4A. Design 4 – bit × 4 – bit binary multiplier using 7483 ICs and minimum number of external NAND gates.

4B. Using 74153 IC and external NAND gates, design the combinational logic circuit to implement following functions:

$F_1(A,B,C) = \overline{A}\overline{B} + AB\overline{C}$

$F_2(A,B,C) = \overline{A} + B$

4C. Explain the significance of asynchronous inputs in a flip flop with a neat logic diagram.

[5+3+2]

5A. Design a self starting synchronous counter to count the BCD digits according to 8 4 -2 -1 code. Use SR – flip flops for the design with minimal external gates.

5B. Design a 4 to 16 decoder using 2 to 4 decoders ONLY.

5C. Design one digit BCD adder using 7483 ICs and NAND gates only.

[5+3+2]