



Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)



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THIRD SEMESTER B.TECH (INSTRUMENTATION & CONTROL ENGINEERING) END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: DIGITAL ELECTRONICS CIRCUITS [ICE 2103]

Time: 3 Hours

MAX. MARKS: 50

Instructions to Candidates:

- ✤ Answer ALL the questions.
- Missing data may be suitably assumed.
- **1A.** Mention any four advantages of digital systems over analog systems.**2**
- **1B.** Reduce the expression f = (B+BC) (B+B'C) (B+D) using Boolean algebra.
- Reduce the following expression using mapping (K map) and implement it using 5 NAND gates.

 $F=\sum m(0,1,2,3,5,7,8,9,10,12,13)$

- 2A. Draw the truth table and obtain the logic expression of a full subtractor. Implement it 5 using the logic gates.
- **2B.** Develop a logic equation for a comparator to compare (A>B) for any two 2 bit **3** numbers A and B.
- **2C.** Differentiate between a multiplexer and a de-multiplexer.
- 3A. With the help of necessary excitation tables and K map reduction, convert a D flipflop to a J-K flip-flop. Draw the logic diagram.
- 3B. Draw the logic diagram of a parallel in parallel out shift register using D flip-flops 3 and explain its working briefly.
- **3C.** Write a note on hazards in asynchronous sequential circuits.
- **4A.** Design and implement a mod-10 asynchronous counter using T flip-flops. **4**
- 4B. Develop a state diagram and primitive flow table for a logic system with 2 inputs, X and Y and one output Z. The logic system changes state on the rising edge of the 2 inputs. Assume initially, X = Y =0; Following table shows the required input output.

x	Y	Z
1	0	1
0	1	0
0	0	No change in output
1	1	No change in output

- 5A. Compare the advantages and disadvantages of programmable logic devices with 2 respect to fixed logic devices.
- **5B.** Show the logic arrangement required to implement a binary full subtractor using the **5** following:
 - i) PROM
 - ii) PLA
- **5C.** Mention any 6 applications of digital electronic circuits.

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