Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

THIRD SEMESTER B.TECH (INSTRUMENTATION & CONTROL ENGG.)

END SEMESTER EXAMINATIONS, NOV/DEC 2015

SUBJECT: DIGITAL ELECTRONICS CIRCUITS [ICE 2103]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Prove that AB'C + A'BC + ABC = A(B + C) using Boolean algebra. **(2M)**

1B. Implement the following expression without further reducing, using only NAND gates. **(3M)**

F= (A + C) (ABC + ACD).

1C. Using the tabular method, obtain the minimal expression for **(5M)**

$f = \sum m (0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$.

2A. Design a logic circuit with 4 inputs A, B, C, D that will produce output '1' only whenever two adjacent input variables are 1's. A & D are also to be treated as adjacent. Implement it using NAND gates. **(4M)**

2B. Design an odd parity bit generator for a 4-bit input. **(3M)**

2C. Implement the following Boolean function using an 8:1 MUX considering D as the input and A, B, C as the selection lines: **(3M)**

F (A, B, C, D) = AB' + BD + B'CD'

3A. The waveforms shown in the Fig.1 are applied to a negative edge – triggered S – R flip flop with active – HIGH PRESET and CLEAR. Draw the output waveform. Assume initially, the output Q is LOW. **(2M)**

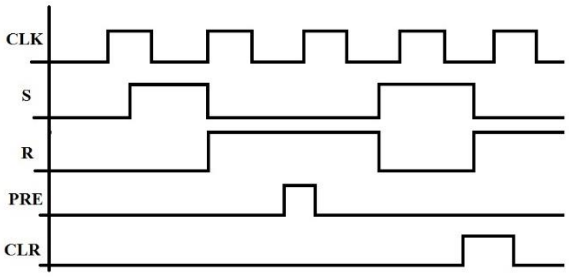

Fig. 1

3B. Explain the working of a parallel-in, serial-out shift register. Also draw the block diagram. **(3M)**

3C. Design a Synchronous 3-bit up-down counter using J-K flip flop. Also draw the state diagram and the logic diagram. **(5M)**

4A. Design a 2-input 2-output synchronous sequential circuit which produces an output z = 1, whenever any of the following input sequences 1100, 1010 or 1001 occur. The circuit resets to its initial state whenever output become 1. Use Mealy model. **(6M)**

4B. Draw an ASM chart and state table for a 2-bit up-down counter having mode control input. **(4M)**

M = 1: Up counting

M = 0: Down counting

The circuit should generate an output 1 whenever the count becomes minimum or maximum.

5A. What do you mean by programmable logic devices? Compare the important features of PROM, PLA and PAL devices. **(3M)**

5B. Determine the size of the PROM required for implementing a single-digit BCD adder/ subtractor with a single control input for selection of operation. **(2M)**

5C. Obtain a primitive flow table for a circuit with two inputs x_1 and x_2, and two outputs z_1 and z_2, that satisfy the following four conditions: **(5M)**

(i) When $x_1x_2 = 00$, the output is $z_1z_2 = 00$.

(ii) When $x_1 = 1$ and x_2 changes from 0 to 1, the output is $z_1z_2 = 01$.

(iii) When $x_2 = 1$ and x_1 changes from 0 to 1, the output is $z_1z_2 = 10$.

(iv) Otherwise, the output doesn't change.

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