Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKE UP EXAMINATIONS, JAN 2016

SUBJECT: ANALOG SYSTEM DESIGN [ELE 208]

REVISED CREDIT SYSTEM

Time: 3 Hours | 13 JANUARY 2016 | MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL** questions.
- Missing data may be suitably assumed.

1A. With neat circuit schematics, develop the expressions for gain, input and output resistances for an op-amp operating in non-inverting mode with negative feedback. (05)

1B. Using a single Op-amps, design a circuit to obtain output voltage $V_O = V_A - V_B - V_C$ .Select feedback resistance Rf = 10 kΩ. (03)

1C. An Op-amp 741 has a slew rate of 0.5V/μsec. Calculate the cut-off frequency for a voltage follower circuit using above op-amp if the peak of sine wave output to be 1V. (02)

2A. Design a practical Integrator whose cutoff frequency in 1 kHz. DC gain is 40 dB. Assume capacitance C = 0.01μF.Hence draw the circuit schematic with all component details. (05)

2B. Design a practical Differentiator to differentiate the signals in the range 1 kHz - 10kHz. Assume suitable capacitance values. Hence draw the circuit schematic with all component details. (05)

3A. Design a square and triangular wave form generator to generate a triangular wave of 4KHz. Derive the expression used. Assume capacitor C=0.01μF and V_{peak} of triangular waveform is 5V. (03)

3B. Design a Schmitt trigger to get the transfer characteristic shown in fig Q3B. Hence draw the output when the input $V_i(t)$=5 sin 314t . Assume the resistance connected across the op-amp terminal and ground is 10KΩ. (04)

3C. With a neat circuit schematic explain the working of precision rectifier. (03)

4A. Design an active second order low pass Butterworth filter circuit with a cut off frequency $1KH_Z$. Assume capacitors of 0.01 μF, if required. (04)

4B. With a neat circuit schematic, explain the working principle of voltage controlled oscillator. Derive an expression to estimate the output frequency. (03)

4C. With a neat circuit schematic explain the working of OP-AMP based log antilog amplifier (03)

5A. Discuss the working of a Phase Locked Loop with suitable block diagram. (04)

5B. Using 555 timer draw the circuit required to generate the waveform shown in Fig 5B. Generate $V_0 2$ form $V_0 1$.Assume Capacitance of 0.1uF (04)

5C. Briefly explain the need for wave shaping circuit in the monostable multivibrator mode. (02)

6A. With a neat circuit diagram, derive the expression for common mode rejection ratio of a emitter coupled differential amplifier (04)

6B. With suitable circuit diagrams, derive expressions for Input and Output Impedance with feedback for a Current Series feedback topology. (04)

6C. List any four characteristics of negative feedback amplifiers. (02)

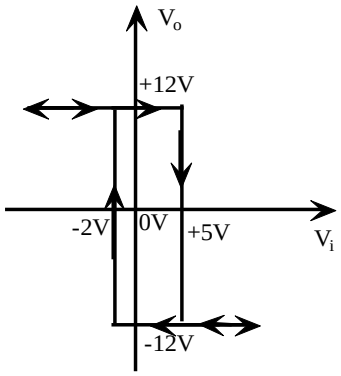

Fig Q.3B.

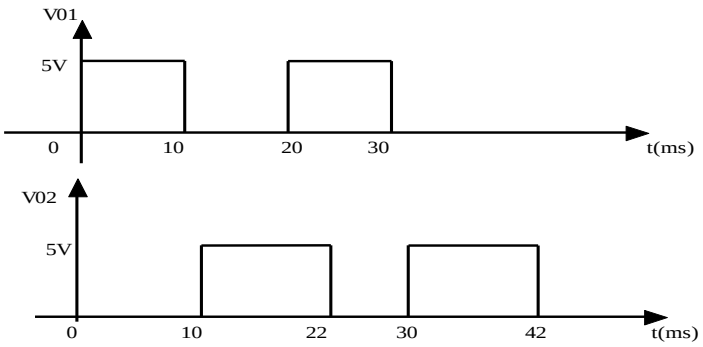

Fig 5B