Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

I SEMESTER M.TECH (PESC)

END SEMESTER EXAMINATIONS, NOVEMBER 2015

SUBJECT: ANALOG AND DIGITAL SYSTEM DESIGN [ELE 509]

REVISED CREDIT SYSTEM

Time: 3 Hours 26 November 2015 MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL** questions.
- Missing data may be suitably assumed.
- DSP Quick reference table may be used.

1A. Design and implement a Butterworth high pass filter with magnitude/frequency response of 3dB attenuation at a frequency of 2KHz and 15dB attenuation at a frequency of 1KHz. **06**

1B. Design and implement 4 bit flash ADC. Take V_{ref}=5V. If V_{in} is 2V find the value of b_1, b_2, b_3 and b_4. **04**

2A. Determine the analog filter transfer function of low pass Chebyshev Type-I filter with the following specifications: A_P= -0.2dB; A_S=-18 dB; Ω_P=10,000 rad/sec; Ω_S=14,000 rad/sec. **06**

2B. Show that the circuit shown in Figure 2B has voltage gain A of the form $A = \frac{V_o}{V_i} = -K\frac{R_2}{R_1}$.

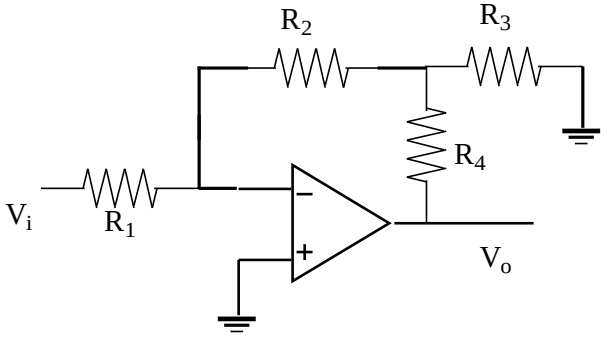

Figure 2B

04

3A. List various operators in VHDL and give their order of precedence. **03**

3B. Design and implement an analog square rooter with the help of analog multiplier. **02**

3C. Draw the state diagram of logic design shown in Figure 3C.

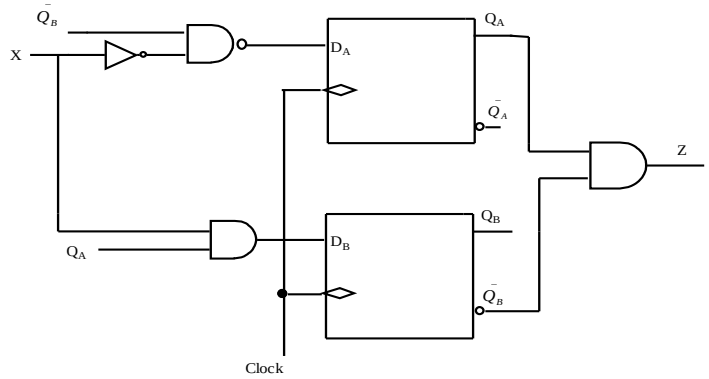

Figure Q3C **05**

4A. Write VHDL code for a 4 bit universal type shift register to do the following operations.

S1	S0	Operations
0	0	Hold
0	1	Shift left by one bit
1	0	Shift right by one bit
1	1	Parallel load

04

4B. Write the VHDL code to generate the sequence 16-8-4-2-1-16-8-4-2-1…… at a frequency of 1 Hz. System clock frequency available is 4.4 MHz. **04**

4C. Translate the following code to a when…else statement.

```
process(a,b,j,k)
    begin
      if a='1' and b='0' then
      step<="0100";
      elsif  a='0' then
      step<=j;
      elsif b='1' then
      step<=k;
      else
      step<="0000";
   end if;
end process;
```

02

5A. Explain the structure of CLB in Xilinx Spartan IIE. **04**

5B. Write a VHDL code for implementing 4:1 Mux using "with select" construct. **03**

5C. Differentiate between signal assignment & variable assignment. **03**

6A. With a block diagram explain the working of PLL. Hence design a frequency multiplier to generate frequency of 1 MHz from input frequency of 1 kHz. **06**

6B. Evaluate the following expression and determine the resulting value.

W= ″01010101", X="1001" , Y="0110", Z="01010100";

(i) K= W or X & not Y xor Z rol 2 (ii) -7 mod -2 **02**

6C. List the merits and demerits of analog active filters compared to passive filters. **02**