Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (DEAC & ME) DEGREE END SEMESTER EXAMINATION NOV/DEC 2015
SUBJECT: ANALOG AND RF VLSI DESIGN [ECE - 503]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Define the following with respect to MOS devices: (i) transconductance (ii) ouput conductance (iii) intrinsic gain. Mention their units. Show that the transconductance of the MOSFET, operated in saturation, (i) increases with the overdrive potential for a given aspect ratio; (ii) decreases with the overdrive potential if I_{ds} is constant.

1B. Find the expression for resistance **Z** for the circuits shown in **FIG. 1B**.

1C. State Miller effect and its usefulness in circuit analysis.

(5+3+2)

2A. Explain the following layout techniques used for analog circuits: [i] interdigitization [ii] symmetry, [iii] common centroid geometry [iv] dummy strip

2B. Derive the expression for small-signal voltage gain and output conductance for the circuit shown in **FIG. 2B**.

2C. Explain the rationale behind half-circuit concept as applicable to differential amplifier.

(5+3+2)

3A. What do you understand by "cascode" topology ? Explain the telescopic PMOS double cascode amplifier with NMOS cascode load. State the merits of the circuit.
Explain the concept of following: [i] simple folded cascode amplifier [ii] folded cascode amplifier with biasing.

3B. Calculate the small-signal voltage gain A_v for NMOS (M_1) CS stage with diode-connected PMOS load (M_2). Given that $(W/L)_1 = 50/1$, $(W/L)_2 = 10/1$, $K_n = 50\ \mu A/V^2$, $\mu_n = 2.5\ \mu_p$ and $I_{ds1} = I_{ds2} = 0.5$ mA. Assume $\lambda = 0$.

3C. Define the following MOS model parameters: [i] γ [ii] Early voltage V_A

(5+3+2)

4A. With a schematic circuit explain the working of an unbalanced CMOS OTA. Give the expression for dominant and non-dominant pole frequency. Bring out the differences between unbalanced and balanced OTA.

4B. Design a double cascode current mirror to sink a current of 10 μA. Find the minimum voltage across the current sink and the output resistance. Given that $K_n = 50\ \mu A/V^2$, $V_{gs} = 1.2$ V, $V_{thn} = 0.83$ V, $V_{thp} = 0.91$ V, $\lambda = 0.06\ V^{-1}$, $V_{DD} = 2.5$ V, $V_{SS} = -2.5$ V.

4C. Explain how the nonlinearity in CS stage is minimized using source degeneration.

(5+3+2)

5A. Discuss the frequency response of common source amplifier by considering high-frequency small signal analysis.

5B. Give the schematic circuit of NMOS common source amplifier with a current mirror active load. Assume all transistors have $W/L = 180\ \mu m/1.8\ \mu m$ and $K_n = 90\ \mu A/V^2,\ K_p = 30\ \mu A/V^2,\ I_b = 0.1\ mA,\ \lambda_n = 0.06\ V^{-1},\ \lambda_p = 0.05\ V^{-1}$. Find the voltage gain and output resistance.

5C. Obtain the expression for small-signal voltage gain for NMOS CG amplifier stage with diode connected PMOS active load for following cases: (i) $\lambda \neq 0, \gamma \neq 0$ (ii) $\lambda = 0, \gamma = 0$

(5+3+2)

6A. With a schematic circuit explain the working and use of Gilbert cell.

6B. For the NMOS differential pair $M_{1,2}$ with a current source load formed using $M_{3,4}$, $(W/L)_{1,2}$ = 15/5, $(W/L)_{3,4}$ = 70/5, $\lambda_n = 0.06\ V^{-1}$, $\lambda_p = 0.05\ V^{-1}$. Given that $\mu_n \approx 2.5\ \mu_p$, K_p= 20 uA/V^2, V_{DD} = -V_{SS} = 2.5 V, R_{bias} = 1.665 MΩ. Find the overall transconductance of the differential amplifier, differential and common-mode small-signal gain for I_{bias} = 10 µA.

6C. Discuss the Layout for resistor and capacitor.

(5+3+2)

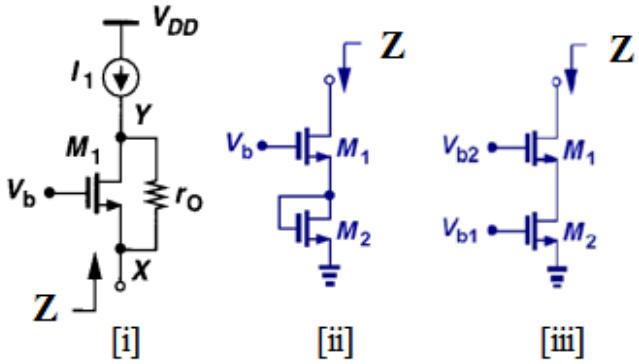

FIG. 1B

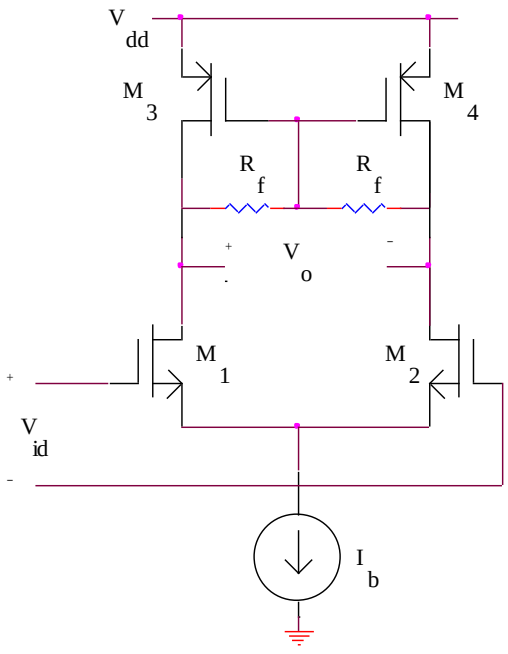

FIG. 2B.