Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (ME) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: ADVANCED DIGITAL VLSI DESIGN (ECE - 521)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Draw neat sketches of cross sectional views of CMOS inverter fabricated using N-well, twin –tub and SOI processes and properly label the regions. Also compare the processes based on the following criteria i) Density of packing ii) susceptibility to latch-up iii) device performance and iv) cost

1B. Derive the expression for the propagation delay of CMOS inverter and show the condition required to achieve symmetry of operation

(6+4)

2A. Draw the circuit and layout for implementing $F= (A.B+C.D)^{/}$ using CMOS logic. Apply Euler path method for obtaining the layout.

2B. Draw the circuit of a functionally complete CMOS D latch and explain the operation with its salient features. Show how you can construct an edge triggered FF using such latches ?

(5+5)

3A. With the help of a neat circuit diagram explain BiCMOS inverter. What are its merits and demerits? Show how you can implement $F= ((A+B+C).D)^{/}$ using BiCMOS logic.

3B. What is meant by general scaling ? Explain. Also illustrate the impact of general scaling on the following parameters: i) Current density ii) Power delay product and iii) Maximum operating frequency

(5+5)

4A. Show the complete circuit of a 4 X 4 NOR based ROM with appropriate decoder circuit to store values 1010, 1101,1001 & 0110. Also compare it with NAND based implementation

4B. Design a full adder circuit using NMOS switches. Using such adder as a block, design a 4 bit ALU and illustrate the operation.

(5+5)

5A. Explain the read and write operations in a 6T SRAM with suitable circuit. Also, discuss the design criteriaand estimate the Cell Ratio and Pull up ratio.

5B. A tapering buffer is used to drive a load capacitance of C_L=15 pF. Suppose the first stage has a C_g of 20fF, calculate the number of stages required ***N***, width factor ***f*** and the delay in terms of τ. Derive the expression used.

(5+5)

6A. With the help of neat diagrams explain clock distribution techniques and compare them

6B. What is meant by di/dt noise? Explain. Also show how it can be reduced.

6C. List the merits and demerits of Dynamic CMOS.

(5+3+2)