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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (DEAC & ME) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: ANALOG AND RF VLSI DESIGN [ECE - 503]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Give the circuit of double cascode current sink. Using small signal ac model, derive the expression for output resistance. What is the minimum output voltage across the current sink?

1B. Apply half-circuit concept to find small-signal differential voltage gain for the circuit given in FIG. 1B. Given that all transistors in the circuit are saturated. Assume $\lambda \neq 0$, $\gamma \neq 0$.

1C. Show that a negative capacitance can be realized using an amplifier block having suitable gain A and a passive capacitance C. State the principle used.

(5+3+2)

2A. Discuss the improved wide-swing cascode current mirror circuits.

2B. In a NMOS source follower circuit with a current sink load, all transistors have W/ L = 100 µm/ 2 µm. Given that I_{bias} =100 µA, η = 0.1, K_n = 75 µA/V^2, K_p = 30 µA/V^2, $r_{ds\text{-}n}$ = 128 kΩ, $r_{ds\text{-}p}$ = 192 kΩ. Find small-signal voltage gain and output resistance.

2C. Define the term single parameter sensitivity. Derive an expression for sensitivity of output current I_o with respect to V_{DD} in a cascode current sink circuit. Give your comments.

(5+3+2)

3A. Give the schematic circuit of a PMOS based folded cascode amplifier. Derive the exact expression for small-signal voltage gain and output resistance. Also give the approximate expression for voltage gain.

3B. Show that the small-signal voltage gain neglecting channel length modulation effect for the circuit shown in FIG. 3B is given by $A_v = 1/(1+\eta)$.

3C. Give the circuit diagram of folded cascade opamp topology and salient features.

(5+3+2)

4A. Show how a variable gain amplifier (VGA) is implemented using differential amplifier. Discuss the two Gilbert cell topologies.

4B. Consider the circuit of nMOS CG amplifier with a pMOS current source load. M_1 is the input MOS device and M_2 is the output MOS of M_2-M_3 current source circuit. Assume that the CG amplifier has a bias current of 0.1mA and that all transistors have a W/L of 100 µm/2 µm. Given that K_n = 50 µA/V^2, K_p = 17 µA/V^2, $g_{ds,n}$ = 10 µmho , $g_{ds,p}$ = 5 µmho, η = 0.1.Compute small-signal voltage gain.

4C. Derive the expression for small-signal common-mode voltage gain in a source-coupled NMOS differential amplifier neglecting second-order effects.

(5+3+2)

5A. Give the CMOS circuit of balanced Operational Transconductance Amplifier? Compare OTA and op-amp with respect to following: [i] area [ii] input and output resistance [iii] gain [iv] bandwidth

5B. Explain the channel length modulation. Derive the expression for channel length modulation parameter (λ).

5C. Discuss the structure of double poly capacitor.

(5+3+2)

6A. Explain the basic PLL block diagram with necessary analog building blocks. Show how PLL can be used for FM demodulation.

6B. With appropriate figures, explain how the differential operation can reduce following: [i] effect of supply noise [ii] Effect of coupled noise from digital clock signal.

6C. State the principle used in the design of RF Mixers.

(5+3+2)

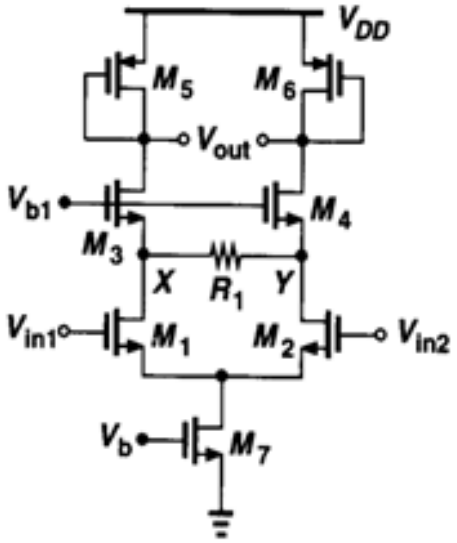

FIG. 1B

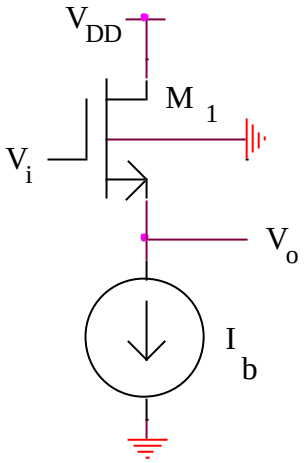

FIG. 3B