Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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FIRST SEMESTER M.TECH. (DEAC & ME) DEGREE END SEMESTER EXAMINATION
NOV / DEC 2015
SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE - 505)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Describe architectural overview of on chip memory of TMS320C62x DSP Processor.
1B. In a coherent multiprocessor scheme, four processors A, B, C, D and E are connected to a memory. Initial content of memory location X is 1. CPU A reads the content of memory location X and then writes 0 to X using write invalidate protocol. With a help of a table, narrate the bus activities and updating of contents in caches of different processors.
1C. Discuss circular addressing mode of a DSP Processor.

(4+4+2)

2A. Describe different methods used, to overcome finite word length effects in a Digital Signal Processor.
2B. Discuss architecture and instructions of a processor, which uses registers for all vector operations except for load and store.
2C. A DSP has a circular buffer. Starting address = 0400h and End address = 040Fh. What are the new values of address pointer of buffer if in the course of address computation, it gets updated to i) 0412h b) 03FCh?

(4+4+2)

3A. A superscalar pipelined machine, capable of fetching and decoding two instructions at a time, having three functional units (F1 & F2 are 2 integer + F3 is a 1 floating point) and having two instances of write back stages.
Given: Ten code segment (C1 to C10)
- C1 requires two cycles to execute
- C3 and C4 conflict for functional unit F3
- C5 depend on value produced by I4
- C5 and C6 conflict for functional unit F2
- C7 and C8 also conflict for functional unit F2
- C9 and C10 conflict for functional conflict for F1

Explain In order Issue, with, in Order completion instruction issue policy to implement the above code.
3B. Write programming model/architecture of a mixed signal microcontroller and discuss any one application.
3C. A 32 bit processor machine has remote memory access time 4000ns. Processors are stalled on remote request and cycle time of processors = 20ns. Base CPI= 6.0 and remote request rate = 0.5% of instructions. Calculate new CPI. Suppose a speed up overall = 100 and speed up enhanced = 200, what fraction of original computation can be sequential? Assume: Parallel with all processors and serial with one processor, in use.

(4+4+2)

4A. Given: The sequence of 5 stage pipelined instructions.

a) I_1 = lw \$1,40 (\$6)
I_2 = add \$6, \$2,\$2
I_3 = sw \$6, 50(\$1)

b) I_1 = lw \$5, -16 (\$5)
I_2 = sw \$5, -16 (\$5)
I_3 = add \$5, \$5, \$5

i) Indicate dependencies and their types

ii) Assume there is no forwarding in this pipelined processor. Indicate hazards and add NOP instructions to eliminate them.

iii) Assume there is full forwarding. Indicate hazards and add NOP instructions to eliminate them.

Show with schematic diagrams.

4B. What is MMU? Explain the following, with necessary diagrams.

i) Different types of page tables.

ii) Different page table entries

Single step page table walk for 1 MB section page translation

4C. Explain Interrupt based I/O strategy with algorithm used for implementation.

(4+4+2)

5A. Build a single cycle data path for implementing combined R –type and memory instructions.

5B. Compare Direct mapped cache, set associative cache and fully associated cache, with necessary examples and diagrams.

5C. Discuss overflow / underflow solutions associated with MAC unit in a DSP Processor.

(4+4+2)

6A. Discuss different types of cache memory optimization techniques.

6B. With regard to parallel architecture of processors, describe

i) SISD ii) SIMD iii) MISD iv) MIMD

Centralized shared Memory architecture vi) Distributed memory architecture

6C. For the following pipelined instructions, with schematic diagram, discuss how program executes if

i) Branch not taken

ii) Branch taken

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20 beq $1, $3, 48
24 sub $12, $2, $5
28 add $13, $6, $2
32 or $14, $2, $2
      .
      .
      .
      .
64 lw $15,$16,$17
68 sub $4, 50 ($7)
72 sw $22, $23, $24
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(4+4+2)