Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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FIRST SEMESTER M.TECH (DEAC & ME) DEGREE END SEMESTER EXAMINATION NOV/DEC 2015

SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE - 505)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Given instruction sequence:

a)
```
lw $1, 40 ($6)
beq $2, $0, Label      ; assume $2 = $0
sw $6, 50 ($2)
add $2,$3,$4
sw $3, 50($4)
```

b)
```
lw $5, -16 ($5)
sw $4, -16($4)
lw $3, -20 ($4)
beq $2, $0, Label      ; assume $2 = $0
add $5,$1,$4
```

For the above code sequence, assume all branches are perfectly predicted and that no delay slots are used. If we only have one memory (for both instructions and data), there is a structural hazard every time we need to fetch an instruction in the same cycle in which another instruction accesses the data. To guarantee forward process, this hazard must be always resolved in favour of instruction that accesses the data. What is the total execution time of this instruction sequence in the five stage pipeline that only has one memory?

1B. What is cache? With regard to ARM cache, explain the following, with necessary diagrams.
i) Different architectures
ii) Virtual cache and physical cache.
iii) Architecture of 8KB cache memory

1C. With a schematic diagram, discuss control hazard for a set of pipelined instructions.

(5+3+2)

2A. Build a single cycle data path for implementing a register format instruction.

2B. What are the different parallel architectures followed in multiprocessors based on instructions and data stream? Explain multiprocessor structures based on memory organizations and their interconnect strategy.

2C. Analyse pipelining adopted in Pentium 4.

(5+3+2)

3A. Write programming model/architecture of MSP 430 microcontroller and discuss it's application.

3B. A superscalar pipelined machine, capable of fetching and decoding two instructions at a time, having three functional units (F1 & F2 are 2 integer + F3 is a 1 floating point) and having two instances of write back stages.

Given: Six code segment (C1 to C6)

- C1 requires two cycles to execute
- C3 and C4 conflict for functional unit F3
- C5 depend on value produced by I4
- C5 and C6 conflict for functional unit F2

Explain different instruction issue policies to implement above code.

3C. Explain Polling based I/O strategy with algorithm used for implementation.

(5+3+2)

4A. Discuss implementation of 8 tap FIR filter using single, two and eight MAC units with necessary diagrams.

4B. Describe architecture of a processor, which uses memory for all vector operations.

4C. Explain reverse carry add addressing mode for 16 point FFT implementation.

(5+3+2)

5A. With regard to ARM MMU, describe the following:

i) Page tables.
ii) Page table entries.
iii) Translation look aside buffer
iv) Single and double Page table walks.

5B. What is the significance of register renaming technique in instruction level parallelism? Explain.

5C. Suppose a speed up overall = 50 and speed up enhanced = 100, what fraction of original computation can be sequential? Assume: Parallel with all processors and serial with one processor, in use.

A 32 bit processor machine with remote memory access time 4000ns. Processor are stalled on remote request and cycle time of processors = 10ns. Base CPI= 2.0 and remote request rate = 0.75% of instructions. Calculate new CPI.

(5+3+2)

6A. Describe architectural overview, memory system of floating point Digital signal processor.

6B. In a coherent multiprocessor scheme, four processors P1, P2, P3, are connected to memory. Initial content of memory location 'M' is 0. CPU P1 reads the content of memory location 'M' and then writes 1 to M. Using different protocols, narrate the bus activities and updating of contents in caches of different processors (in table form).

6C. Discuss how output of one pipeline is directly released into another pipeline with an for implanting the equation CV + Z (where C is a scalar constant and V & Z are vectors)

(5+3+2)