Reg. No.										

MANIPAL UNIVERSITY

FIRST SEMESTER ME EMBEDDED SYSTEMS / THIRD SEMESTER MSc. TECH EMBEDDED SYSTEMS DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: ESD 607 – COMPUTER ARCHITECTURE

Wednesday, November 25, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1A. List out the difference between combinational and sequential Logic Circuits.

1B. Define the following with suitable examples:

i) Minterms

ii) Maxterms

(5 marks × 2 = 10 marks)

2. In a computer instruction format the instruction length and size of the address field are 11 & 4 bits respectively. A computer architect has already designed 6 two address & 24 zero address instructions. What is the maximum number of 1 address instructions that can be added to the instruction set?

(10 marks)

3. Using a 4 – bit CLA as the building block, design the fastest 64 – bit adder. Estimate the add time of your design.

(10 marks)

4. Design a 4 - bit general purpose register as follows:

S1	S0	FUNCTION
0	0	Load external data
0	1	Rotate left ($A_3 \leftarrow A_0$, $A_i \leftarrow A_{i-1}$ for i = 1, 2, 3)
1	0	Rotate right ($A_0 \leftarrow A_3$, $A_i \leftarrow A_{i+1}$ for i = 0, 1, 2)
1	1	No operation

(10 marks)

5. Explain the Booth's algorithm for multiplication of two numbers represented in 2's complement form for 3 x -3.

(10 marks)

6. Consider the following register transfer description:

Declare registers A [8], B [8], C [8], N [4];

Declare bus Outbus [8];

START: A ← 1, B ← 1, C ← 0; N ← 10;

LOOP: If N = 0 then go to HALT;

C ← A + B;

A ← B;

B ← C;

N ← N-1;

Go to LOOP;

Outbus ← A;

Outbus ← B;

HALT: HALT

Propose a block schematic of the optimized microprogrammed control unit; provide the state diagram and obtain the control words required in the optimized control memory.

(10 marks)

7. Explain the register banking in ARM7.

(10 marks)

8. Explain the processor modes of ARM7.

(5 marks × 2 = 10 marks)

9. Explain the working of following instructions:

9A. STMIA r0!, {r2, r3, r4}

9B. ADDEQ r0,r1,r2,LSR#2

9C. MRS CPSR,r0

9D. MOV PC,r14

9E. BIC r0,r1

(2 marks × 5 = 10 marks)

10. Describe High performance Bus master in Advance Micro-controller Bus Architecture.

(10 marks)