Reg. No.										

MANIPAL UNIVERSITY

FOURTH SEMESTER MSc. TECH EMBEDDED SYSTEMS/THIRD SEMESTER MSc. TECH EMBEDDED & INSTRUMENTATION (ESIGELEC, FRANCE) DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: ESD 608 / ESI 605 – EMBEDDED SYSTEMS DESIGN

(REPEATERS)

Thursday, November 26, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1A. Explain different stages involved in a product development starting from need to product launch.

1B. For a particular product, you determine the NRE cost and unit cost to be the following for three listed IC technologies:

Technology	NRE Cost in ₹	Unit Cost in ₹
FPGA	5,000	25
ASIC	50,000	10
VLSI	300,000	5

Determine the precise volumes for which each technology yields the lowest total cost.

(8+2 = 10 marks)

2. Design a 3-bit counter that counts the following sequence: 1, 3, 7, 5, 2, 6, 1, 3… etc. This counter has an output "ODD "whose value is one when the present count value is odd. Use the sequential logic design. Start from a state diagram, draw the state table, minimize the logic and draw the final circuit.

(10 marks)

3. Starting from the program, obtain a data path for the calculation of GCD of two integers. Also indicate all control signals in the data path.

(10 marks)

4. With reference to ADC, bring out the significance of:

4A. Resolution

4B. Sampling frequency

4C. Output type

4D. Input type

4E. Clock frequency with suitable examples

(2 marks × 5 = 10 marks)

Reservation table for function X

	0	1	2	3	4	5	6	7
S1	X					X		X
S2		X		X				
S3			X		X		X	

Reservation table for function Y

	0	1	2	3	4	5
S1	Y				Y	
S2			Y			
S3		Y		Y		Y

(2+2+4+2 = 10 marks)

10. Optimize the reservation table shown in Fig.Q.10 find:

10A. Forbidden Latencies

10B. Collision Vector

10C. State diagram with all state transitions

10D. Percentage of efficiency of the system with and without optimization. Show the calculations.

	0	1	2	3	4
S1	X				X
S2		X		X	
S3			X	X	

Fig.Q.10

(1+1+4+4 = 10 marks)

5. With the suitable figure explain:

5A. Direct

5B. Set Associative

5C. Fully Associative mapping techniques and compare them

(3+3+4 = 10 marks)

6A. Explain the address translation using TLB. What are the advantages and disadvantages of this scheme?

6B. The following measurements are obtained from a computer system that uses memory system with a TLB:

- time taken to conduct an associative search in the TLB = 160 nsec.
- main memory access time = 1μsec.
- Determine the average access time assuming a TLB hit ratio of 80%.

(8+2 = 10 marks)

7. The size of the virtual address space = 8 k words
Size of the physical address space = 2k words
Page size = 512 words
The page request sequence is: 0,1,2,3,5,6,3,4,7,2,6,5.

7A. Calculate the number of physical and virtual pages.

7B. Calculate value of "h" for the above sequence in case of Direct mapping.

7C. Find all the virtual addresses that generate page fault after the end of the above sequence.

(2+4+4 = 10 marks)

8A. Explain the three internal forwarding techniques with suitable examples.

8B. Apply internal forwarding technique for the following sequence of instruction to obtain one instruction using the graphical representation.

R0 ⟵ (M1)
R0 ⟵ (R0) + (M2)
R0 ⟵ (R0) * (M3)
M4 ⟵ R0

(6+4 = 10 marks)

9. For the given reservation tables for function X & Y compute the following:

9A. Forbidden latencies for X & Y

9B. Collision Vector Cx & Cy

9C. State diagram for X & Y

9D. MAL for X & Y

Reservation table for function X

	0	1	2	3	4	5	6	7
S1	X					X		X
S2		X		X				
S3			X		X		X	

Reservation table for function Y

	0	1	2	3	4	5
S1	Y				Y	
S2			Y			
S3		Y		Y		Y

(2+2+4+2 = 10 marks)

10. Optimize the reservation table shown in Fig.Q.10 find:

10A. Forbidden Latencies

10B. Collision Vector

10C. State diagram with all state transitions

10D. Percentage of efficiency of the system with and without optimization. Show the calculations.

	0	1	2	3	4
S1	X				X
S2		X		X	
S3			X	X	

Fig.Q.10

(1+1+4+4 = 10 marks)