Reg. No.										

MANIPAL UNIVERSITY

FOURTH SEMESTER MSc. TECH (VLSI DESIGN) DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: EDA 604 – ADVANCED VLSI DESIGN

Thursday, November 19, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1A. Explain the effect of Temperature and Voltage on CMOS capacitor.

1B. For a 1pF poly1-poly2 capacitor at room temperature (27°C), estimate the minimum and maximum capacitance over a temperature range of -40 to 100°C.
[Data Given: TCC = 20ppm/°C]

(5+5 = 10 marks)

2. Draw and explain the circuit of Cascode current mirror and show that output resistance of the Cascode current mirror $\mathbf{R_o = r_o(1+g_m r_o)+r_o}$, where $\mathbf{r_o}$ is output resistance of all the MOSFETs, $\mathbf{g_m}$ is the transconductance of all the MOS used in the circuit.

(10 marks)

3. With a diagram, explain ***cascode current mirror***. What are its advantages over a simple current mirror?

(10 marks)

4. How can we maximize the voltage gain of a CMOS Common-Source amplifier with passive resistor load? What are the different trade-offs that should be done? Obtain the expression for the gain considering channel-length modulation.

(10 marks)

5. Compare simple *Resistor-Only*, *Resistor-MOSFET* and *MOSFET-Only* voltage dividers with diagrams. What is their major common drawback?

(10 marks)

6. Explain, with the help of a neat schematic diagram, a bandgap voltage reference. What are the advantages of this circuit over other simple references?

(10 marks)

7. For the differential amplifier shown in Fig. 7, calculate the slew rate and the small-signal upper 3dB frequency. Assume bottom zero bias capacitance.

[Data given: V_{DD} = 5V, R1 = 380K, C_L = 2pF, I_{SS} = 20μA, C_J = $1.04*10^{-4}$, CGDO = $3.8*10^{-10}$, W/L of M1, M2, M3, M4, M5 and M6 are 15/5, 15/5, 70/5, 70/5, 15/5 and 30/5 respectively, length of the drain implant = 6μm.]

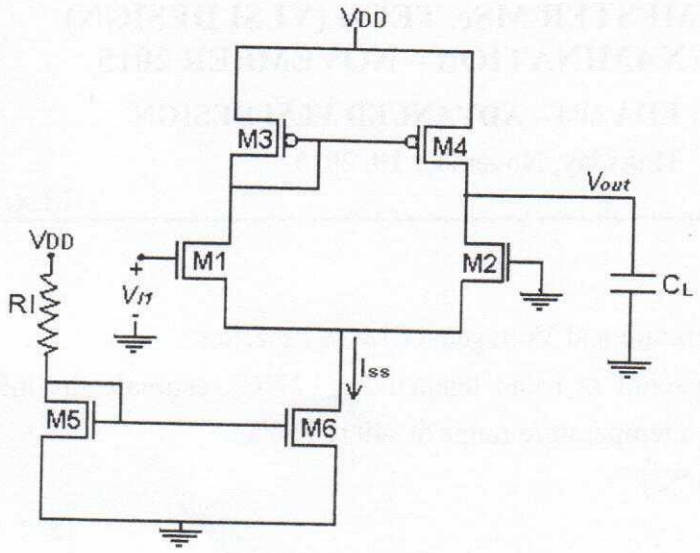

Figure 7

(10 marks)

8. Explain, with an example, how to make *switched-capacitor* circuits insensitive to stray capacitances.

(10 marks)

9. Discuss the different errors that occur in a Sample-and-Hold circuit.

(10 marks)

10. With diagrams, explain the principle of working of the Two-Step ADC. What are the accuracy issues related to it?

(10 marks)