Reg. No.										

MANIPAL UNIVERSITY

FOURTH SEMESTER MSc. TECH (VLSI DESIGN/EMBEDDED SYSTEMS) DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: EDA 602 / ESD 602 – DIGITAL SIGNAL PROCESSING

Saturday, November 21, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

Answer ALL questions.

1. Explain Radix-2 DIF-FFT algorithm with N = 8. Comment on number of complex multiplication and addition.

(10 marks)

2. Realize the following system functions using Direct form-I, Direct form-II and Cascade and Parallel forms

$H(z) = [0.8 / (1 + 0.2z^{-1} + z^{-2})] + [1.0 / (1 - 0.5z^{-1} + z^{-2})]$

(10 marks)

3. The desired amplitude response of a certain FIR filter with linear phase is

$|H(e^{jf})| = 1$; for $f \geq 500$ Hz

$|H(e^{jf})| = 0$; elsewhere

The sampling frequency $f_s = 2$ kHz and the impulse response is to be 5.5 mSec long. Design the filter using frequency-sampling technique.

(10 marks)

4. Design a low-pass filter using windows that will have 3-dB cutoff at 30π rad/sec and an attenuation of 50 dB at 45π rad/sec. The filter is required to have linear phase characteristics and the system employs a sampling frequency of 100 Hz.

(10 marks)

5. A lowpass filter specification is given as

Passband: $0 \geq |H(e^{j\Omega})|_{dB} \geq -1$ $\quad 0 \leq \Omega \leq 20$ rad/sec

Stopband: $|H(e^{j\Omega})|_{dB} < -60$ $\quad \Omega \geq 200$ rad/sec.

Let sampling period be = 0.01 sec.

Design a digital Chebychev filter using Bilinear Transformation. Realize the Filter.

(20 marks)

6. Provide the direct-form FIR filter structures of decimator and interpolator. What are the problems in the implementation? How do you overcome these problems? Also provide the linear phase structure.

(10 marks)

7. Explain how multirate signal processing can be used in the analysis and synthesis of speech signals in subband coding technique.

(10 marks)

8. Explain analytically, how optimum filter coefficients are obtained on Mean Square Error sense in Wiener Noise Canceller Configuration.

(10 marks)

9. Explain how a higher throughput is obtained using the VLIW architecture. Give an example of a DSP that has VLIW architecture. What does instruction-pipelining mean? Explain how pipelining increases the throughput efficiency.

(10 marks)