Reg. No.										

MANIPAL UNIVERSITY

FIRST SEMESTER ME VLSI DESIGN DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: EDA 615.7 – CAD FOR VLSI (ELECTIVE 1)

Wednesday, November 25, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1. Describe various entities for optimization in VLSI design.

(10 marks)

2. Briefly describe various stages and tools in Algorithmic and System Design.

(10 marks)

3. Discuss the important verification methods.

(10 marks)

4. Explain the array and time-wheel representations of the event queue in event driven simulation.

(10 marks)

5A. Explain the applications of partitioning in high level synthesis.
5B. Describe the cluster growth method of partitioning.

(4+6 = 10 marks)

6. Describe the task of scheduling w.r.t. the following:

6A. Functional units with varying delays
6B. Multi-functional units

(7+3 = 10 marks)

7. What is floor-planning? Describe floor plan based design methodology and its merits.

(3+7 = 10 marks)

8. Explain Lee's algorithm for area routing with an example.

(10 marks)

9A. What are the applications of layout compaction?
9B. Discuss about the layout compaction design rules.

(5+5 = 10 marks)

10. Construct the BDD, using the variable ordering $A \leq B \leq C \leq D$ for the following function:
$F = ABC + A'B'C' + AB'C + ACD$

(10 marks)