Reg. No.										

MANIPAL UNIVERSITY

FIRST SEMESTER ME VLSI DESIGN DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: EDA 613 – DIGITAL SYSTEMS AND VLSI DESIGN

Wednesday, November 18, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1. Explain the possible crystal defects and their effects after the crystal is grown.

(10 marks)

2. Explain SOI process with neat diagrams.

(10 marks)

3. Describe the various photoresist performance factors.

(10 marks)

4. Explain the concept of diffusion. Write a note on dopant sources.

(10 marks)

5. With diagrams, compare NELT, NELS and HMOS static load inverters.

(10 marks)

6. State and prove a theorem specifying the condition for zero short-circuit power consumption in a CMOS gate.

(10 marks)

7. What is a structured CMOS design? What are its advantages? Explain the steps in this design with an example.

(10 marks)

8. Design a 4:1 multiplexer:

8A. Using a combination of CMOS switches and logic gates.

8B. Using only CMOS logic gates.

Assess the efficiency of each implementation by counting the total number of switches used in each implementation. Which is more efficient? Why?

(5+5 = 10 marks)

9. Design a CMOS inverter for which the inverter threshold is half the V_{DD} and have equal rise time (t_r) and fall time (t_f).

(10 marks)

10A. Explain with an example, dynamic CMOS logic. What are the advantages and drawbacks of a simple dynamic CMOS logic?

10B. What is zipper CMOS logic? Explain with neat diagrams.

(5+5 = 10 marks)