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# MANIPAL UNIVERSITY

## FIRST SEMESTER ME VLSI DESIGN / FOURTH SEMESTER MSc. TECH EMBEDDED SYSTEMS DEGREE EXAMINATION – NOVEMBER 2015

### SUBJECT: EDA 611/ESD 616.1 (ELECTIVE 2) – HIGH LEVEL DIGITAL DESIGN

Monday, November 23, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1. Design 32x1 multiplexer using 4x1 multiplexers.

(10 marks)

2. Design and explain D-FlipFlop with synchronous and asynchronous reset.

(10 marks)

3. Design a 0110 sequence detector using Moore Machine.

(10 marks)

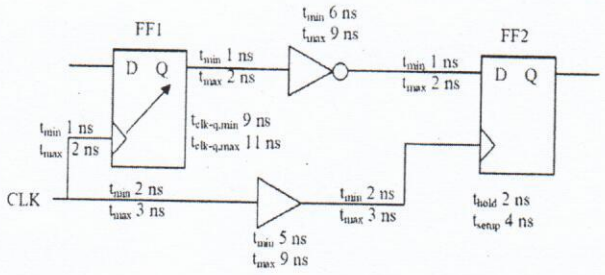
4. Design the 4-bit Comparator which determines if A less than B, A greater than B, A equal to B.

(10 marks)

5. Design the carry look ahead adder.

(10 marks)

6. In the following circuit, find out whether there is any Setup or Hold Violation.




(10 marks)

7. Design a dual port synchronous memory with neat diagram.

(10 marks)

8. Explain LAB Structure in Altera FPGA.

(10 marks)

9. Explain the AHB Master read and write operations using timing diagrams.

(10 marks)

10. Design Real Time Clock with following features:

10A. Display – Year : Month : Day

10B. Clock freq 300 KHz

(10 marks)