Reg. No.										

MANIPAL UNIVERSITY

FIRST SEMESTER ME VLSI DESIGN DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: EDA 615.5 – SYSTEM-ON-CHIP DESIGN (ELECTIVE 1)

Wednesday, November 25, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1. Explain the functionalities of VLIW processors.

(10 marks)

2. Explain the functionalities of Multiprocessors.

(10 marks)

3. Explain briefly about post-partitioning analysis in ESL flow.

(10 marks)

4. What are different types of cache organization? Explain them with neat diagrams.

(10 marks)

5. Explain strategies for line replacement at "miss time".

(10 marks)

6. Explain the following terms:

6A. USB bus driver

6B. USB root hub

(5+5 = 10 marks)

7. Explain the following terms:

7A. USB bus interface layer

7B. USB device layer

(5+5 = 10 marks)

8. Explain the basic concepts in processor micro-architecture.

(10 marks)

9. Explain the following terms:

9A. Bimodal dynamic branch prediction

9B. Two – level adaptive dynamic branch prediction

(5+5 = 10 marks)

10. Explain in detail about dynamic networks in Network On Chip.

(10 marks)