Reg. No.										

MANIPAL UNIVERSITY

FIRST SEMESTER ME VLSI DESIGN DEGREE EXAMINATION – NOVEMBER 2015

SUBJECT: EDA 617 – VERIFICATION

Friday, November 20, 2015

Time: 10:00 – 13:00 Hrs. Max. Marks: 100

1. What is Testbench? Explain the any Five importance of verification.

(10 marks)

2. What is Functional Verification? Explain with respect to Black-Box Verification.

(10 marks)

3. Explain the Event driven simulation with an example.

(10 marks)

4. Explain the code coverage with an example.

(10 marks)

5. Explain with neat diagram, application of different levels of verification.

(10 marks)

6. Explain the following in systemVerilog with an example:

6A. Packed Array
6B. Unpacked array
6C. Union
6D. Queues

(2½ marks × 4 = 10 marks)

7. Bring out the difference between the following:

7A. Fork/join
7B. Fork/join_any
7C. Fork/join_none
7D. Fork/join disable

(2½ marks × 4 = 10 marks)

8. What is self-checking? Explain with an example.

(10 marks)

9. Explain directed stimulus with an example.

(10 marks)

10. What is transaction level modeling and explain its characteristics.

(10 marks)