Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
(A Constituent Institute of Manipal University)
Manipal – 576 104

V SEMESTER B.Tech (BME) DEGREE MAKE-UP EXAMINATIONS , DEC/JAN 2015-16
SUBJECT: MICROPROCESSORS (BME 307)
Monday, January 04, 2016 (2.00 p.m. - 5.00 p.m.)

TIME: 3 HOURS **MAX. MARKS: 100**

Instruction to Candidates:

Answer any FIVE full questions.
Assume relevant data if missing.
Give diagrams wherever necessary.

1A.	Sketch the programmer's model of the 8086 & the 68000 microprocessors.	2+2
1B.	What is the provision available in the 68000 microprocessor to handle hardware interrupts? What is the order of hardware interrupt priorities? How do you mask the interrupts?	4+2+2
1C.	Make a list and write function of the 8086 microprocessor signals specific to the maximum mode of operation.	8
2A.	It is required to arrange 100 bytes available in the data segment of the 8086 system memory, in ascending order. Write an appropriate assembly language program.	10
2B.	Write an 8086 assembly language program to read a single digit number from the keyboard and display its ASCII code in the standard output device.	6
2C.	Write a MACRO function for the 8086 microprocessor to display a character string in the standard output device.	4
3A.	When and how the 68000 microprocessor enters into address error exception processing?	4
3B.	Draw the logic-diagram of the "RESET" logic associated with the 8284 Clock generator and draw a practical RESET circuit.	2+2
3C.	List and explain with illustrations, different types of CALL and RET instructions supported by the 8086 microprocessor.	8+4
4A.	Identify the operations carried out by the 8086 instruction "MOV AX, DS:1125H", and depicting all bus control signals, sketch corresponding bus cycle timing diagram. Assume that the processor is in the minimum mode of operation.	8
4B.	An 8086 microprocessor system requires the following memory and I/O devices: (i) Two 1KB EPROM chips (ii) Two 2KB SRAM chips, and (iii) One 8255 PPI chip Design an address decoder to interface above devices in the memory map of the 8086, and allocate address to each device such that the design meets the RESET requirement of the microprocessor.	12

5A. How do you make use of the hardware interrupt "NMI" of the 8086 for: 5+5

(i) Detecting power failure, and

(ii) To generate longer time-delay.

5B. Design an 8086 microprocessor based hardware, and write an appropriate assembly language program, to generate a triangular waveform of frequency 1KHz and amplitude +5V. 10

6A. What is the provision available in the 68000 microprocessor to synchronize itself with the 6800 peripherals? Explain. 4

6B. Write the operation and significance of the following 8086 instructions: 2×4 = 8

(i) XLAT

(ii) CBW

(iii) STD

(iv) AAD

6C. How do you increase the driving capability of the address and the data bus of the 8086 microprocessor system? Explain with the help of appropriate interfacing devices. 4+4