MANIPAL INSTITUTE OF TECHNOLOGY

(A Constituent Institute of Manipal University)
Manipal – 576 104

FIFTH SEMESTER B. Tech (BME) DEGREE END-SEM EXAMINATIONS – NOV. / DEC. 2015
SUBJECT: MICROPROCESSORS (BME 307)
Wednesday, December 02, 2015 (2.00 p.m. - 5.00 p.m.)

TIME: 3 HOURS **MAX. MARKS: 100**

Instruction to Candidates:

Answer any FIVE full questions.
Assume relevant data if missing.
Give diagrams wherever necessary.

1A. What are the advantages of the 68000 microprocessor over the 8086 microprocessor? 4

1B. How do you initiate auto-vectoring in a 68000 microprocessor system? Illustrate with an appropriate circuit. 8

1C. Identify the pins specific to the microprocessors' the 8086 and the 68000, in the list given below, and write the function and significance of each pin. 2×4 = 8

(i) ALE

(ii) $\overline{FC0}, \overline{FC1}, \overline{FC2}$

(iii) $\overline{TEST}$

(iv) $MIN / \overline{MAX}$

2A. It is required to find out the square root of a 2-digit hexadecimal number present in a memory location in the data segment of the 8086 system. Write an assembly language program to display the number and its square root if it is a perfect square; if not display a message "NOT PERFECT SQUARE". 10

2B. Write an 8086 assembly language program to find the sum of hundred 2-digit BCD numbers present in an array in the data segment. Store the sum in the next consecutive memory location. 6

2C. Write a procedure for the 8086 microprocessor to convert a 2-digit hexadecimal number present in BL register into ASCII code. 4

3A. What happens if the following instruction sequence is executed in the 68000 microprocessor? Write the response of the microprocessor. 4

```
MOVE.L #$012436
ADD.B (A1)+, D0
MOVE.W D7, (A1)
```

3B. Draw the logic-diagram of the "READY Logic" associated with the 8284 Clock generator and sketch READY & RDY timing diagrams. 2+2

3C. Read the 8086 assembly language program given below and answer the following questions: 2+4+6

(i) What is the operation carried out by the main program and the procedure?

(ii) Debug and make a list of syntactic & logical errors in the program.

(iii) Write the corrected, memory efficient executable version of the same program.

```
MAIN:  MOV CX, 100
       LEA SI, SRC_LOC
       LEA DI, DEST_LOC
       CLD
  UP:  REP MOVSB
       PUSH AL
       CALL PROD
       STOSB
       LOOP UP
       HLT

PROD:  MOV CL, 05
       XOR AL, AH
       MOV AH, AL
       POP BX
ABVE:  ADD AL, BL
       JNC  DOWN
       ADC AH, 00
       DEC CL
DOWN:  JNZ ABVE
       RET 02
```

4A. Depicting all bus control signals, sketch a labelled 8086 minimum mode memory write bus cycle timing diagram with 3 WAIT states. 8

4B. An 8086 microprocessor system requires the following memory and I/O devices: 12

(i) Two 4KB EPROM chips
(ii) Two 2KB EPROM chips
(iii) Four 1KB SRAM chips, and
(iv) Two 8255 PPI chips

Design an address decoder to interface above devices in the memory map of the 8086, and allocate address to each device such that the design meets the RESET and Interrupt requirements.

5A. M/s ABCD Pvt. Ltd is planning to automate the product counter in the assembly line of their manufacturing unit capable of producing 75 finished products per day. Design an 8086 microprocessor based product counter which updates the counts in a standard output device. 10

5B. Design an 8086 microprocessor based hardware, and write an appropriate assembly language program, to digitize the Lead-II ECG (in the monitoring range) over 1 minute duration. 10

6A. Why is the bus cycle of the 68000 microprocessor asynchronous? How do you terminate the bus cycle? Design a logic circuit to have a bus cycle with four T-states. 1+2+3

6B. Write the operation and significance of the following instructions of the 8086 microprocessor. 4+4

(i) AAA

(ii) SAL

6C. How do you separate the address and the data available on the multiplexed Address/Data bus of the 8086 with the help of an interfacing device? Explain with relevant diagrams. 6