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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIFTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2015
SUBJECT: VLSI DESIGN [ECE 305]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Missing data may be suitably assumed.

1A. Derive pull-up to pull-down ratio (Z_{PU}/ Z_{PD}) for an NMOS inverter driven by another NMOS inverter through enhancement type NMOS pass transistor.

1B. Explain the condition leading to the channel pinch-off in an NMOS device with an appropriate figure.

1C. Calculate I_{ds} and V_{ds} for the circuit shown in FIG. 1(C). Given that K_n= 200 μA/V^2, V_{thn}= 0.6 V, $W/L = 3$ for transistor M1.

(5+3+2)

2A. Identify whether the given logic as ratioed or non-ratioed: [a] Pseudo-NMOS [b] Clocked CMOS. Give the circuit implementation of logic function $Z = \overline{A_1.A_2.A_3 + B_1.B_2}$ using single-phase dynamic CMOS logic and explain the working. State any two merits and demerits of single-phase dynamic CMOS.

2B. Sketch a transistor-level schematic for a depletion load NMOS logic gate for each of the following functions: (i) $Y = \overline{ABC}$ (ii) $Y = A \oplus B$ (iii) $Y = \overline{(AB + C(A+B))}$

2C. Given that V_{DD} = 1.2 V and V_{th} = 0.4 V. Determine V_{out} in FIG. Q2(C) for the following: (i) V_{in} = 0.6 V (ii) V_{in} = 0.9 V [Neglect the body effect]

(5+3+2)

3A. Explain the steps involved in the twin-tub fabrication process.

3B. Explain Latch-up in CMOS and suggest remedies for the same.

3C. Consider a pair of cascaded CMOS inverters each having appropriate L: W ratios chosen such that the inverter has equal rise and fall time. Show the inverter pair delay calculation for rising and falling step input.

(5+3+2)

4A. Calculate the capacitances C_{in} and C_{out} for the structure shown in FIG. 4(A). Neglect peripheral capacitance. Refer Table A for area capacitance values.

4B. With a truth table, give the NMOS gate based implementation of SR latch using only NAND gates.

4C. With CMOS implementation of Positive D latch using TGs, explain the working.

(5+3+2)

5A. Give the mixed stick notation and explain in brief the working of 4-bit right shift NMOS dynamic shift register with required control inputs. Give the layout for 1/2-bit NMOS shift register cell.

5B. Explain the working of 6-T SRAM.

5C. Bring out the differences between constant E field scaling and constant voltage scaling. Find the scaling effect of these models on Gate oxide capacitance per unit area C_{ox} .

(5+3+2)

6A. Discuss the structured design approach as applied to N+1-bit even/ odd parity generator. The output of parity generator P is 1 (0) for even (odd) number of 1s at input. Give the stick notation for NMOS based implementation of the standard cell.

6B. Explain following terms with illustration/ example: [i] Regularity [ii] Structured design approach and leaf cell.

6C. Give the BiCMOS circuit implementation of [i] Two input NAND gate [II] Two-input NOR gate.

(5+3+2)

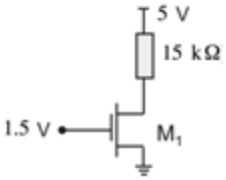

FIG. 1(C)

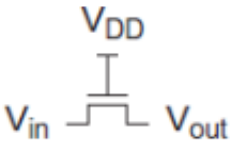

FIG. Q2(C)

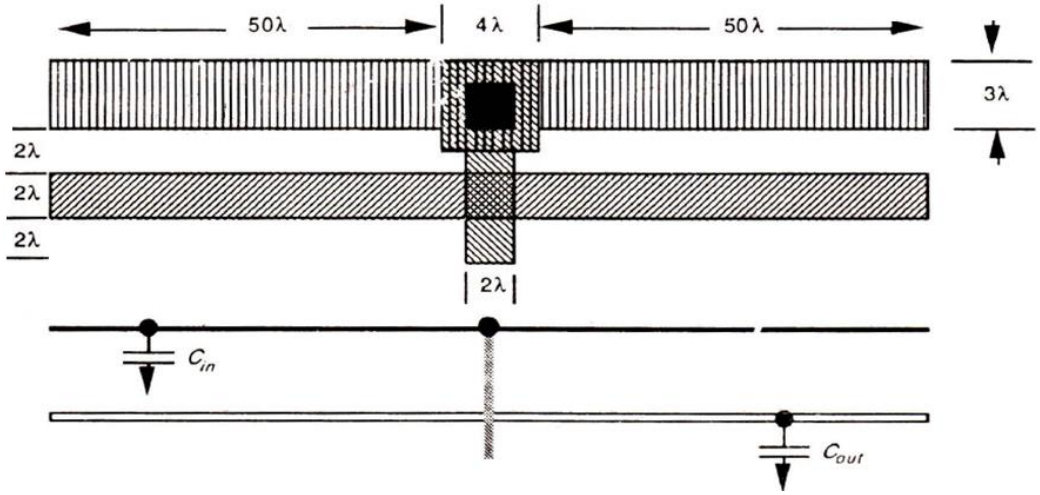

FIG. 4(A)

Table A Typical values of area capacitance for 5 µm technology

Capacitance	Value in $10^{-4}\mathrm{pF}/\mu\mathrm{m}^{-2}$	Relative value
Gate-to-channel	4	1.0
Diffusion	1	0.25
Poly-to-substrate	0.4	0.1
Metal1-to-substrate	0.3	0.075